

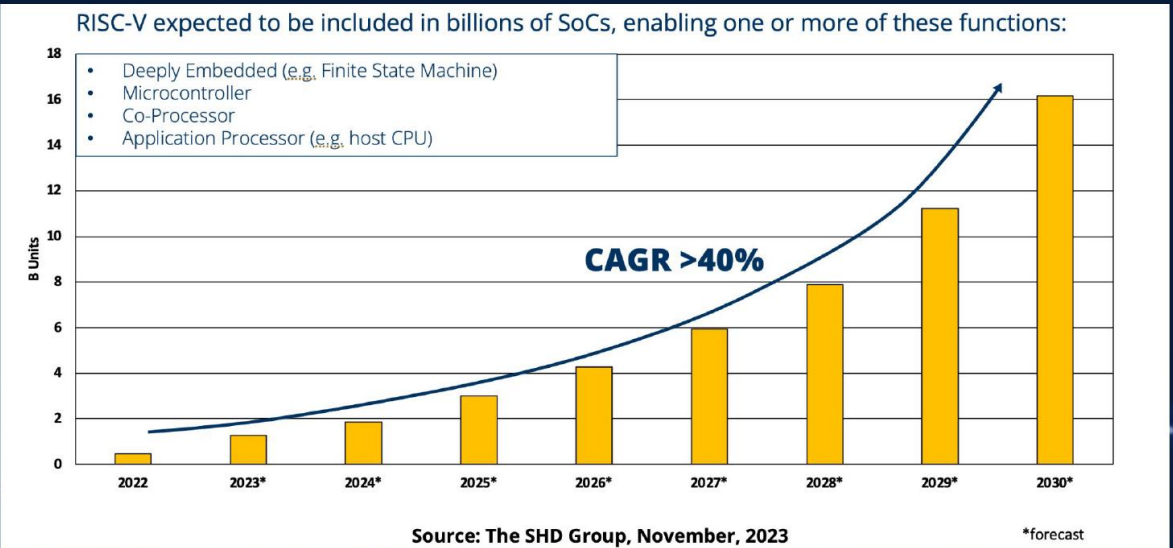
BREAKING THE RISC-V MCUs ECOSYSTEM BARRIERS

RISC-V SUMMIT EUROPE 2024
RENESAS ELECTRONICS CORPORATION

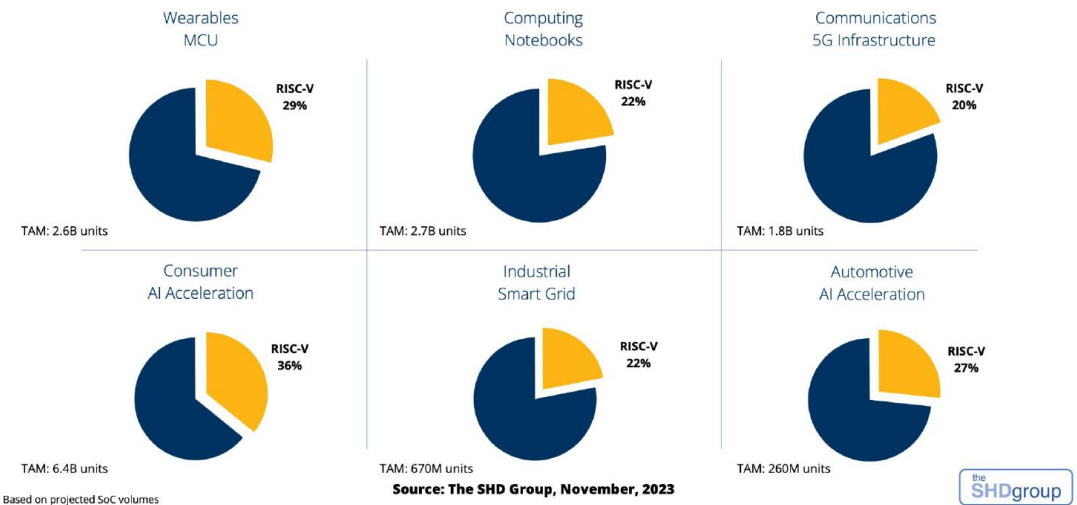
AGENDA

- RISC-V snapshot
- Embedded developers' challenges
- Breaking the barriers
- Renesas RISC-V MCU hardware and ecosystem details
- Summary

RISC-V will be in more than 16 billion SoCs by 2030



Selected Market Share Projections for RISC-V in 2030



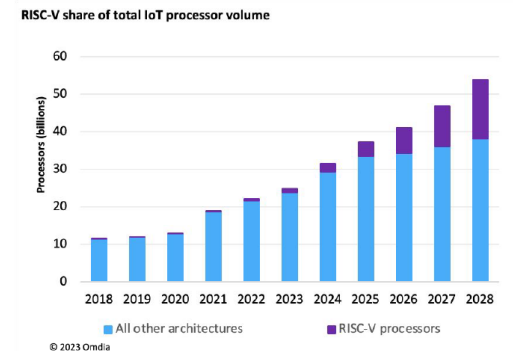
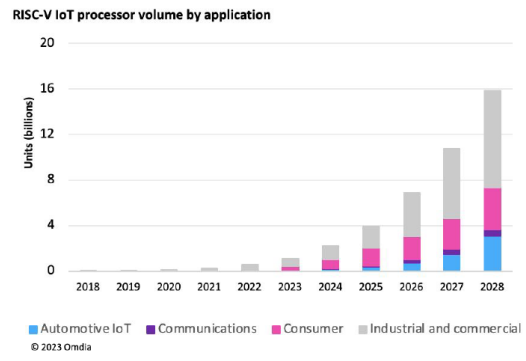
More than 4,300 RISC-V Members across 70 Countries



- 108 Chip**
SoC, IP, FPGA
- 4 Systems**
ODM, OEM
- 3 I/O**
Memory, network, storage
- 17 Industry**
Cloud, mobile, HPC, ML, automotive
- 21 Services**
Fab, design services
- 170 Research**
Universities, Labs, other alliances
- 51 Software**
Dev tools, firmware, OS
- >3900 Individuals**
RISC-V engineers and advocates

RISC-V membership up 28% in 2023

RISC-V is showing amazing growth in IoT



- RISC-V IoT processors grew at roughly 150% compound annual growth rate (CAGR) between 2018 and 2023.
- From 2023 through 2028, the growth rate is expected to top 75% per year.
- In 2018, RISC-V processors accounted for just 0.1% of processors in the IoT. By 2028, that figure should approach 30%.

Source: Omdia, RISC-V in the IoT - 2023 Analysis

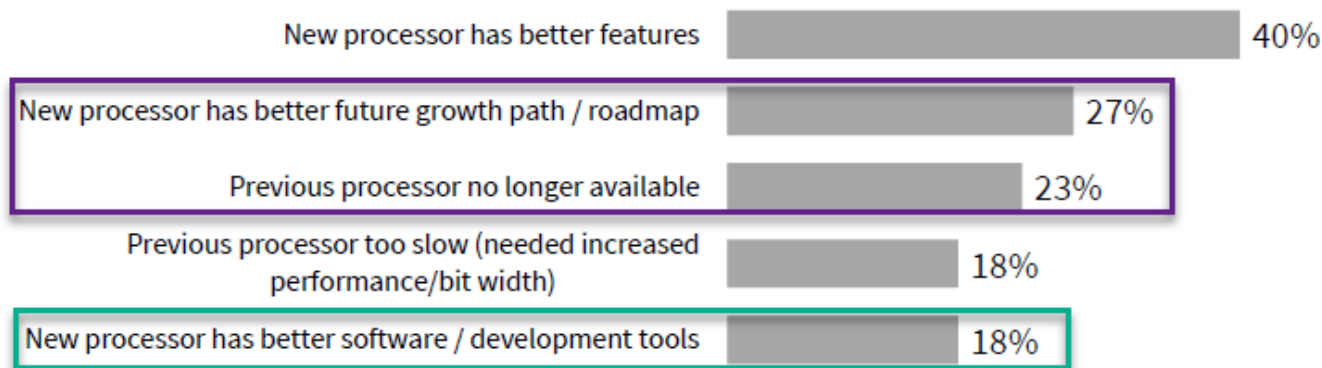
RISC-V is inevitable – „welcome to the open era of computing“

DEVELOPER'S CHALLENGES

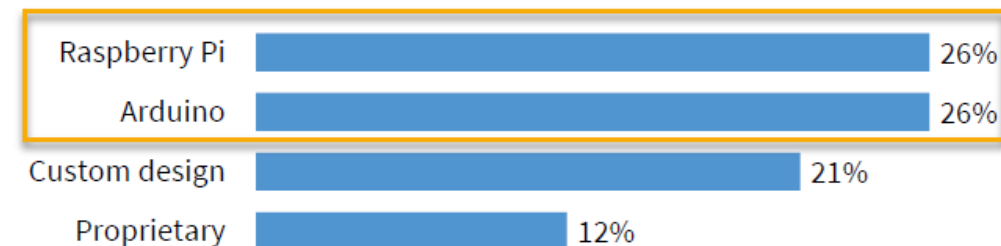
EMBEDDED DEVELOPMENT CHALLENGES WITH A PERSPECTIVE ON RISC-V OPPORTUNITIES

- ~55% of projects are incremental upgrades: add software features and/or better MPUs/MCUs (particularly in larger OEMs).
 - Main areas: industrial automation & instrumentation, IoT, communications, automotive. ~1/3 is related to IoT (sensor driven, industrial or mobile comms applications).
- C language still dominates. “Improved debugging process” top design challenge in near future. Usage of Raspberry Pi and Arduino for proof-of-concept development is popular (~52% use).
- Among those changing processors, ~54% chose a processor from a different family, **architecture or instruction set**.

Reason for Switching Processors



Board Used in Current Design(s)



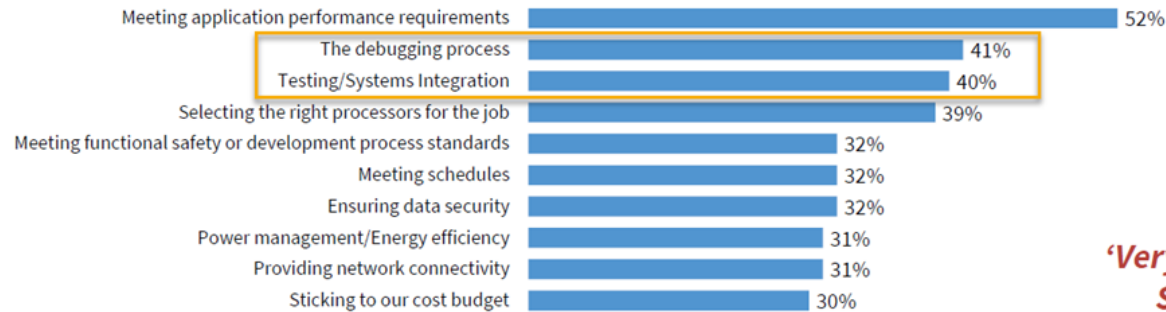
Courtesy of Aspencore, „Embedded Survey: The current state of embedded development, 2023“, www.embedded.com

EMBEDDED DEVELOPMENT CHALLENGES WITH A PERSPECTIVE ON RISC-V OPPORTUNITIES

- Among obvious application requirements, most perceived challenges are **debug, integration and test**.

Meeting performance specs, processor choice and test/debugging are critical issues

Safety, security and power management are also high on the agenda (especially for EMEA and APAC designers)

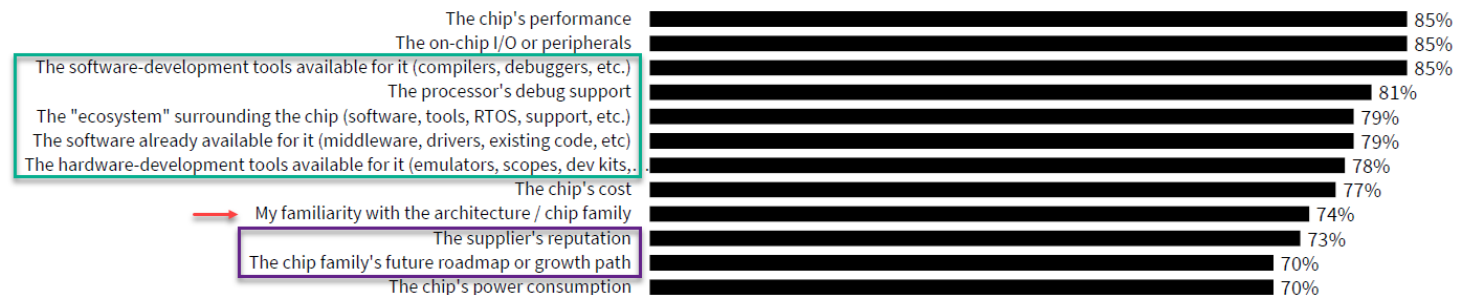


'Very Important' Summary

Courtesy of Aspencore, „Embedded Survey: The current state of embedded development, 2023“. www.embedded.com

Processor selection involves weighing many interrelated factors

Performance, available peripherals, HW/SW tool environment, support ecosystem, and other issues are high on developer agendas



- The “ecosystem” (IDEs, software, toolchain, development tools) **plays a dominant role**
- Choices in terms of architecture/chip family tend to be ‘sticky’
- **Broad commercial support and reliable sourcing** are important

CONCERNS AND ADOPTION BARRIERS FROM A MICROCONTROLLER USER PERSPECTIVE



BREAKING THE BARRIERS

SUPPORTING THE RISC-V GROWTH

The ecosystem is key

Renesas is engaged in developing the RISC-V ecosystem

- Provide free of charge IDE, compiler, configuration/debug/programming tools.
- Partner with market-leading suppliers of commercial debuggers, production programmers, software, IDEs.
- Continue expanding partner and solution network (hardware platforms, software stacks etc.)

Ease the migration

Crush adoption barriers!

- World-wide availability of low-cost development kit, MCU samples, application notes, training and support.
- Configuration and driver generation tool abstracts architectural details. Users can focus on the application.
- Establish RISC-V as open platform for next-generation non-proprietary solutions.

Reliable sourcing

Need for renowned suppliers

- Renesas leading the market with innovation, ready for the RISC-V momentum.
- Prove RISC-V commercial microcontroller products with excellent quality AND long term support.
- Support 8/16-bit mature designs migration to 32-bit at higher performance and lower cost.

RENESAS RISC-V MCU

HARDWARE AND ECOSYSTEM DETAILS

RISC-V GENERAL PURPOSE MCU

128KB FLASH WITH 16KB RAM

- 110-nm low power, low leakage process
- Wide operating temperature range:
Ta = -40°C to 125°C
- Wide Operating Voltage: 1.6V - 5V

Highlights:

- Renesas own CPU design
- High performance core (3.88 CM/MHz*)
- Rich set of analog and digital interfaces
- Small packages: QFN 48/32/24, WLCSP16
- Lots of safety and protection features
- Fast startup

*IAR Compiler

R9A02G021

48MHz 32-bit RV32I [MACB]

CLIC | cJTAG

<div style="border-bottom: 1px solid #ccc; padding: 5px;">Memory</div> <ul style="list-style-type: none"> Code Flash 128 KB SRAM 12 KB ECC SRAM 4KB DataFlash 4KB 	<div style="border-bottom: 1px solid #ccc; padding: 5px;">Analog</div> <ul style="list-style-type: none"> 12-bit A/D x 10 ch Comparator (2ch) Temperature Sensor DAC (2ch) Internal VREF 	<div style="border-bottom: 1px solid #ccc; padding: 5px;">Timer</div> <ul style="list-style-type: none"> TAU 16-bit (8 ch) Interval timer 32-bit (8-bit, 4ch) WDT RTC 	<div style="border-bottom: 1px solid #ccc; padding: 5px;">HMI</div> <ul style="list-style-type: none"> KINT
<div style="border-bottom: 1px solid #ccc; padding: 5px;">Communication</div> <ul style="list-style-type: none"> SAU (6 ch) I2C x 2 LP-UART x2 REMC 	<div style="border-bottom: 1px solid #ccc; padding: 5px;">System</div> <ul style="list-style-type: none"> DTC Interrupt Controller Clock Generation On-Chip Oscillator HOCO / MOCO / LOCO ELC Low-power Modes Clock output TRNG Current control High current pins 	<div style="border-bottom: 1px solid #ccc; padding: 5px;">Safety</div> <ul style="list-style-type: none"> SRAM Parity Check SRAM ECC Clock monitor CRC IWDT 32-Bit DOC ADC self test Boot swap (startup area select) 	<div style="border-bottom: 1px solid #ccc; padding: 5px;">Protection</div> <ul style="list-style-type: none"> Unique ID Customer ID Flash read protection Flash shield protection
<div style="border-bottom: 1px solid #ccc; padding: 5px;">Package</div> <ul style="list-style-type: none"> QFN 48,32, 24 (QFP 32,48) WLCSP 16 			

<https://www.renesas.com/r9a02g021>

RENESAS RISC-V CPU

FEW IMPLEMENTATION DETAILS

CPU performance and safety features

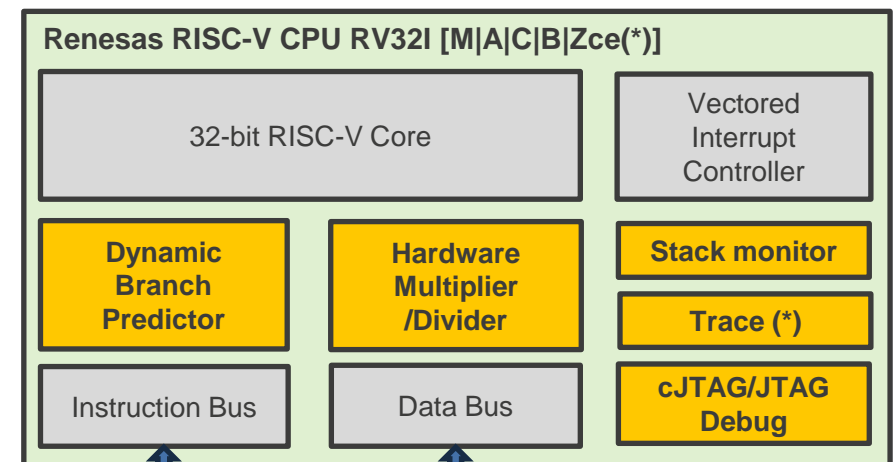
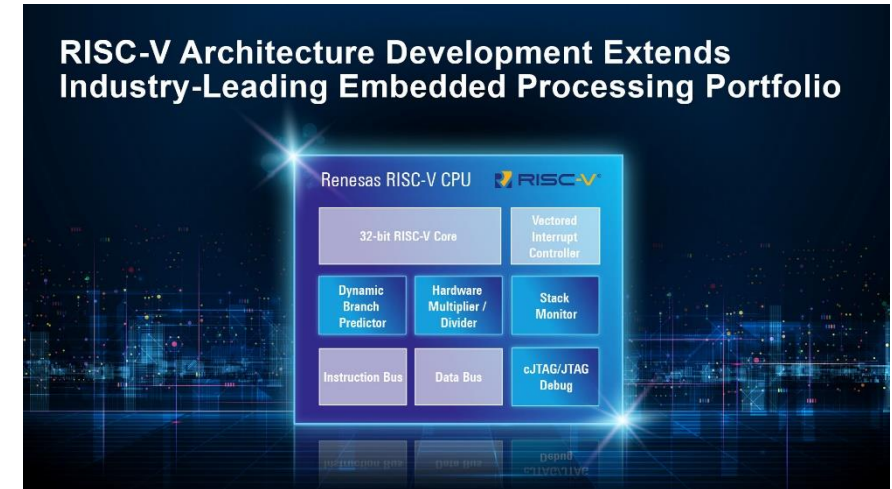
- **RV32I** + **M**(ultiply), **A**(tomic), **C**(ompressed), **B**(it-manipulation), **Zce**(*) extensions
- Single issue in-order 2-stage, with dynamic branch predictor.
- Most instructions execute in 1 cycle
- Little endian, Machine mode, Misaligned access not supported
- Stack overflow detection to detect pointer overflow during stack save/restore
- Performance monitors: cycle and instruction count registers, machine timer
- Achieve fast CPU context switch via register banks for save/restore (*)

Interrupt controller

- Core Local Interrupt Controller (CLIC) with 32 interrupts, 16 interrupt levels
 - Selective hardware vectoring with priority preemption, NMI support

Debug

- Debug/Transport Module (DM, DTM), 4 hardware breakpoint registers
- Trace module for program flow tracing (*)

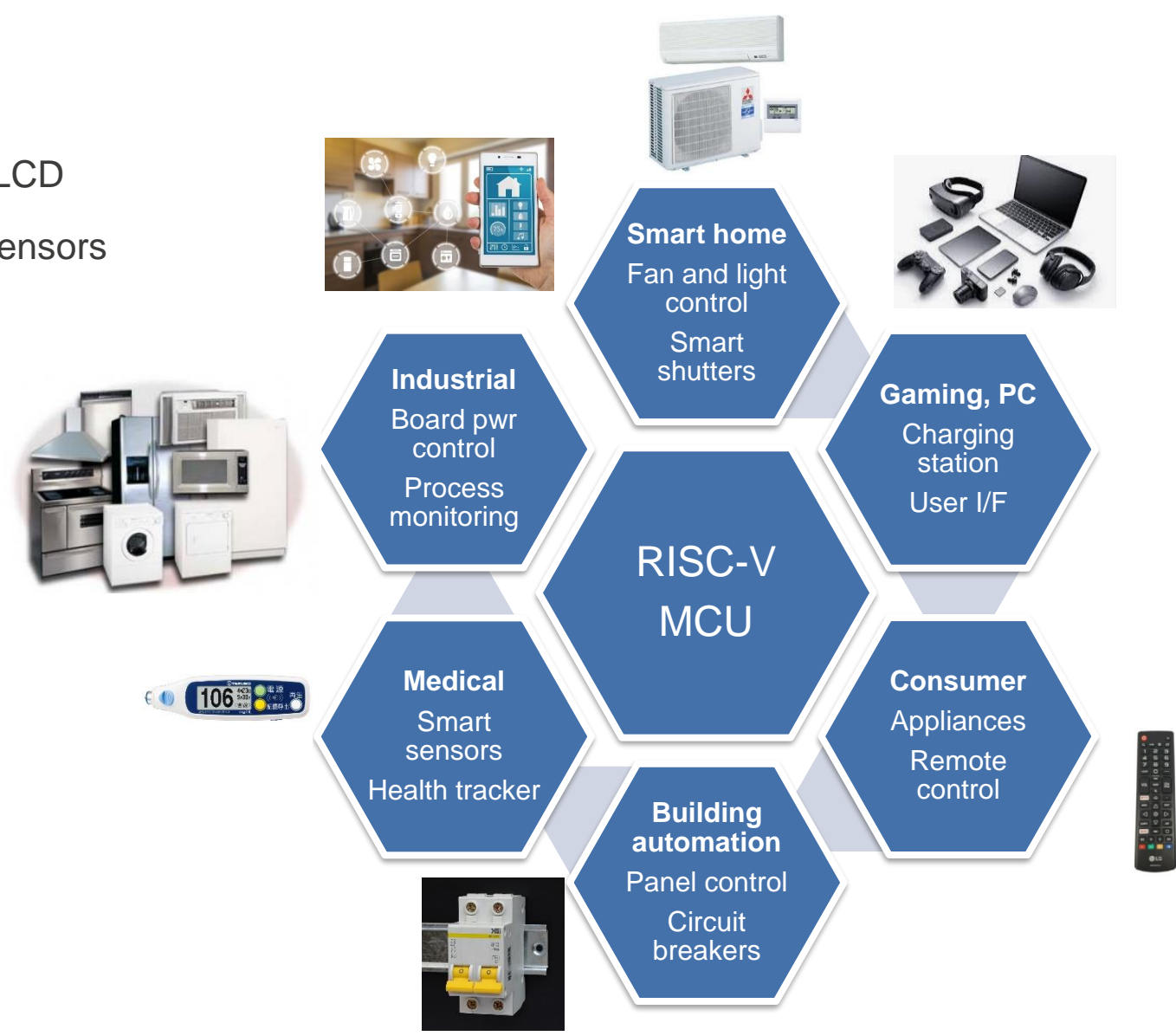


(*) not in first product implementation

32-BIT RISC-V MCU

MARKETS AND APPLICATIONS

- Consumer electronics, home appliances w/ or w/o LCD
- Industrial sensors, sensor modules, bus powered sensors
- Medical sensors, health tracking
- Remote controls, battery powered applications
- Low power home accessories, detectors
- Vehicle tracking
- Intelligent power supplies, inverters
- AND MANY MORE...
- Early customer evaluations ongoing.



RISC-V MCU DEVELOPMENT ENVIRONMENT

BROADLY SUPPORTED AND EASY TO USE

On-Chip Debug

- Renesas E2 & E2 Lite



- SEGGER J-Link



- IAR I-Jet



- Opella-XD



IDE

- Renesas e² studio



- SEGGER Embedded Studio



- IAR Embedded Workbench



- RiscFree SDK



Compiler

- LLVM
llvm-gcc-renesas.com



- SEGGER RISC-V compiler



- IAR RISC-V Compiler

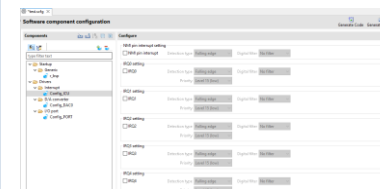


- Integrated toolchain

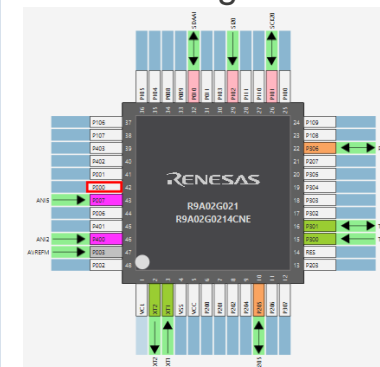


Support Tools

- Smart Configurator



- Pin configurator



- Standalone versions for IAR and SEGGER IDE

Kits and Boards

- Evaluation Kits



FPB-R9A02G021 with Jlink-OB

SMART CONFIGURATOR

QUICK AND NON-EXHAUSTIVE TOUR

<https://www.renesas.com/us/en/software-tool/risc-v-smart-configurator>

GUI environment for generating driver code that handles the details of chip startup and peripheral modules settings.

The screenshot displays the Smart Configurator interface, divided into two main sections: "Clocks configuration" and "Software component configuration".

Clocks configuration: This section includes a block diagram and several configuration panels. The "Operation mode" is set to "High-speed mode", "Type setting" is "Type A", and "VCC setting" is "2.7 V ≤ VCC ≤ 5.5 V". The block diagram shows connections for an external clock input (20 MHz), a sub-clock oscillator (32.768 kHz), a high-speed on-chip oscillator (48 MHz), and a middle-speed on-chip oscillator. The diagram also shows the resulting clock outputs: System clock (ICLK) at 48 MHz, Peripheral module clock (PCLKB) at 24 MHz, and CKOCR (CKODIV[2:0]) at x1/4. Other outputs include CACMCLK/TML32MCLK/UARTAMCLK and CACMOCLK/TML32MOCLK/UARTAMOCLK.

Software component configuration: This section shows a tree view of components under "Components". The "Configure" panel is open for "Config_UART1". The "Transmission" tab is active, showing settings for "UART1 clock setting" (Operation clock: CK00, Clock source: PCLKB, Clock frequency: 24000 kHz), "Transfer mode setting" (Single transfer mode selected), "Data length setting" (8 bits selected), "Transfer direction setting" (LSB selected), "Parity setting" (None selected), "Stop bit length setting" (1 bit selected), "Transfer data level setting" (Non-reverse selected), "Transfer rate setting" (115200 bps, Current error: 0.16%), and "Interrupt setting" (Transmit end interrupt priority: Level 15 (low)). The "Callback function setting" section has "Transmission end" checked.

Select clock sources, configure and make connections in the block diagram

Add sw modules, setup peripherals, check for errors, switch the channels for use by drivers of multi-channel modules

SMART CONFIGURATOR

QUICK AND NON-EXHAUSTIVE TOUR

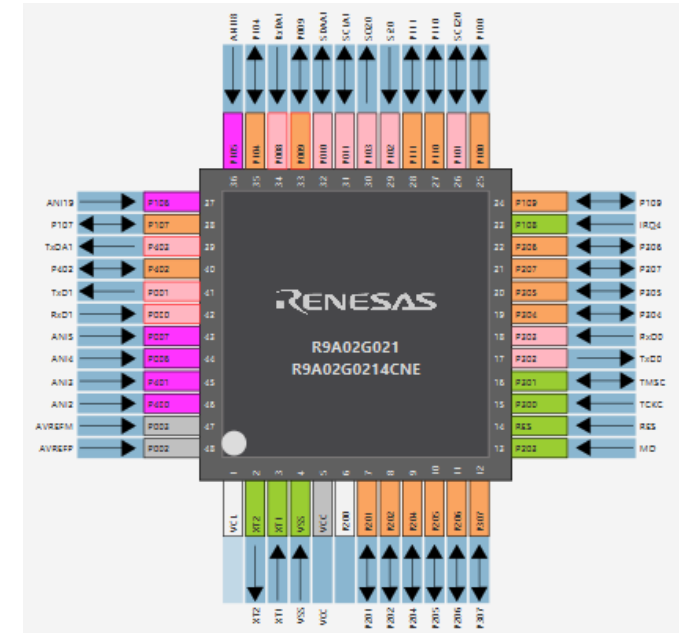
The screenshot shows the 'Pin configuration' interface with 'Hardware Resource' and 'Pin Function' tabs. The 'Pin Function' tab contains a table with the following data:

Enabled	Function	Assignment	Pin Number	Direction	Remarks
<input checked="" type="checkbox"/>	SCLA0	P102/T101/TO01/SCLA0/SI20/SDA20/RxD2/IRQ2	28	IO	
<input checked="" type="checkbox"/>	SDAA0	P103/T102/TO02/SDAA0/SO20/TxD2	17	IO	

Display pin function options, assign pins per each peripheral module, check consistency and resolve pin multiplexing conflicts automatically

- Developer Assistance
 - Config_PORT
 - Config_UART1
 - void R_Config_UART1_Create(void)
 - void R_Config_UART1_Start(void)
 - void R_Config_UART1_Stop(void)
 - MD_STATUS R_Config_UART1_Send(uint8_t * const tx_buf, uint16_t tx_num)
 - MD_STATUS R_Config_UART1_Receive(uint8_t * const rx_buf, uint16_t rx_num)
 - void R_Config_UART1_Loopback_Enable(void)
 - void R_Config_UART1_Loopback_Disable(void)
 - void R_Config_UART1_Create_UserInit(void)
 - Usage example

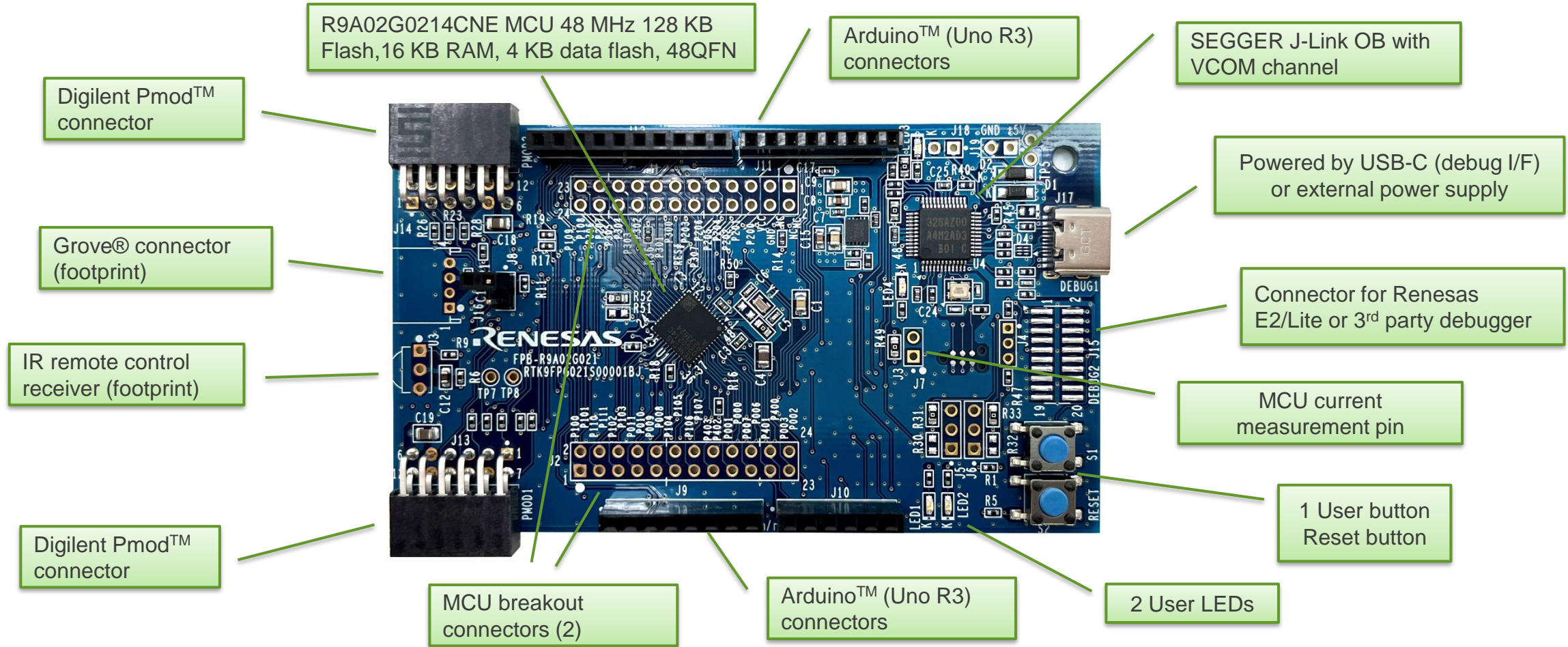
Drag and drop code snippets from the project manager
Browse API manual



Display and assign symbolic names, check allocation status easily by color codes

FPB-R9A02G021

RISC-V MCU FAST PROTOTYPING BOARD



renesas.com/fpb-r9a02g021 (User manual, quick start guide, development tools, schematics, design files & example projects)
RTK9FPG021S00001BJ (Orderable part number. Available at broad market catalog distributors)

SUMMARY

SUMMARY

Renesas leads the market and is RISC-V ready

- **Renesas high quality and support** ensures your RISC-V based MCU commercial success.
- **This MCU is an ideal choice for market leaders** which value non-proprietary ISAs like RISC-V.
- The innovative **Renesas RISC-V CPU** enables **efficient applications**, with **cost advantages** thanks to **rich feature set**

Easy development, low cost, with broad tools support

- Users can avoid upfront investments and **develop free of charge** using the Renesas tools.
- **Commercial support from industry tools leaders** like IAR, SEGGER, and a steadily expanding ecosystem.
- **Smart Configurator** tool mitigates the concern of learning the new ISA
- The **low-cost board** delivers an affordable and pleasuring out-of-the-box user experience.
- Application level support with extensive **documentation** and **software programming examples**

[Renesas.com](https://www.renesas.com)

