RISC-V SUMMIT EU
JUNE 24 – 28 | MUNICH 2024

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

RISC-V@BSC: Fostering RISC-V strategy in Europe through Research, Innovation & Education

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EXCELENCIA SEVERO OCHOA
MINISTERIO DE CIENCIA E INNOVACIÓN
AGENCIA ESTATAL DE INVESTIGACIÓN

MareNostrum

BSC

Booth 17

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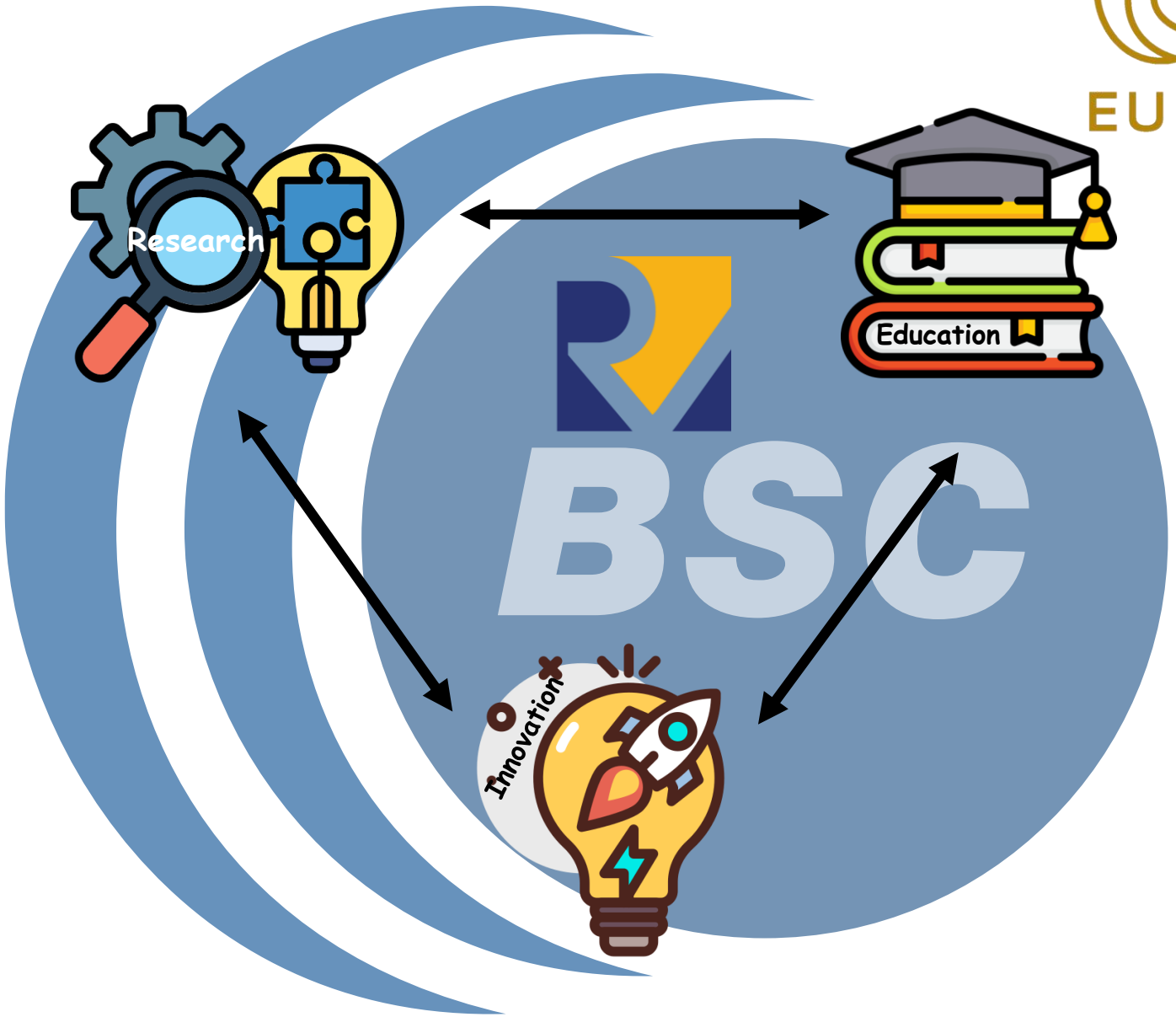
Computer Sciences

RISC-V@BSC: R&i&E



European Commission

EuroHPC Joint Undertaking

MINISTERIO DE CIENCIA E INNOVACIÓN

AGENCIA ESTATAL DE INVESTIGACIÓN

EURO²

CASTIEL 2

SOHA

TRAINING

RESEARCH

INNOVATION

BETC

RISC-V

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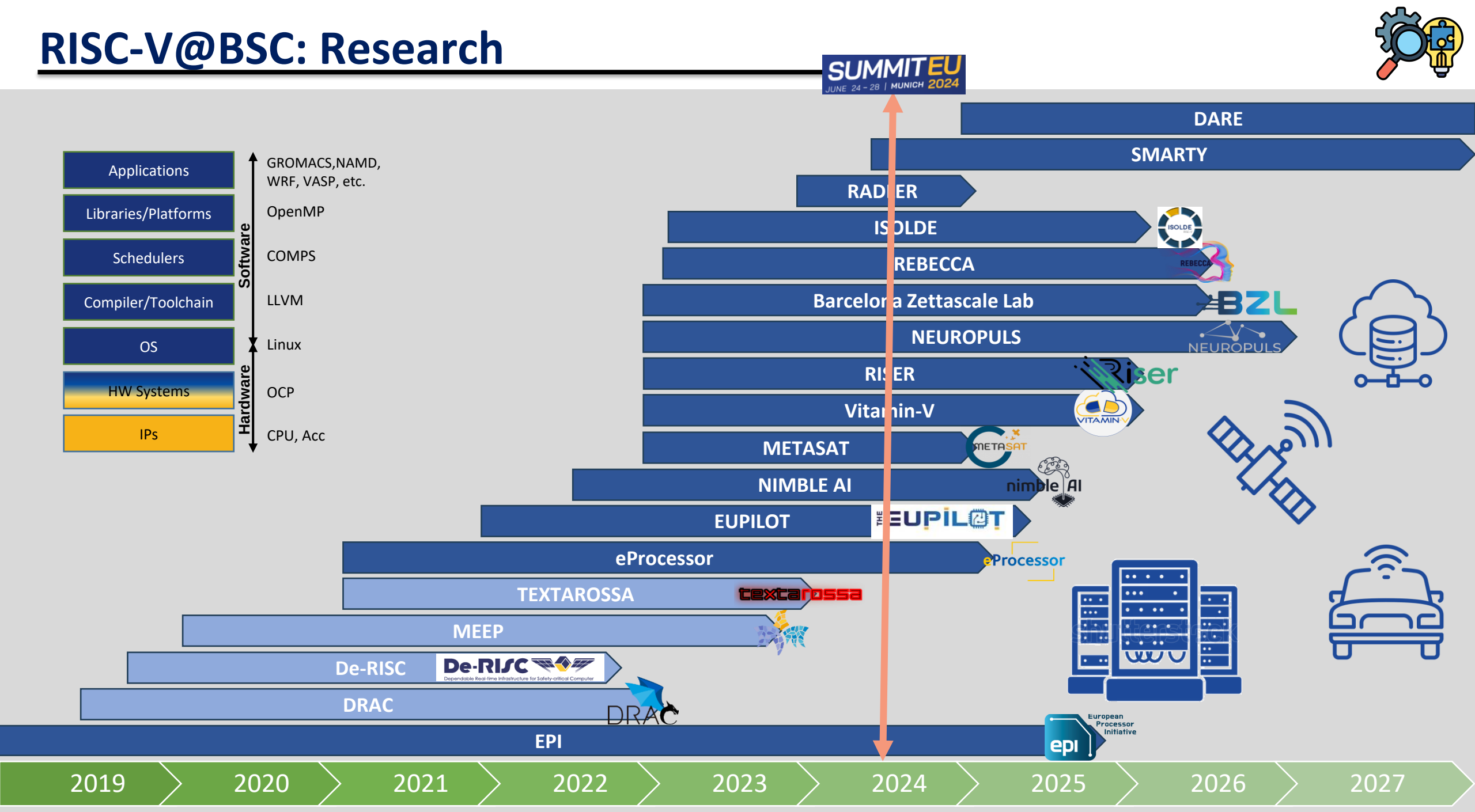
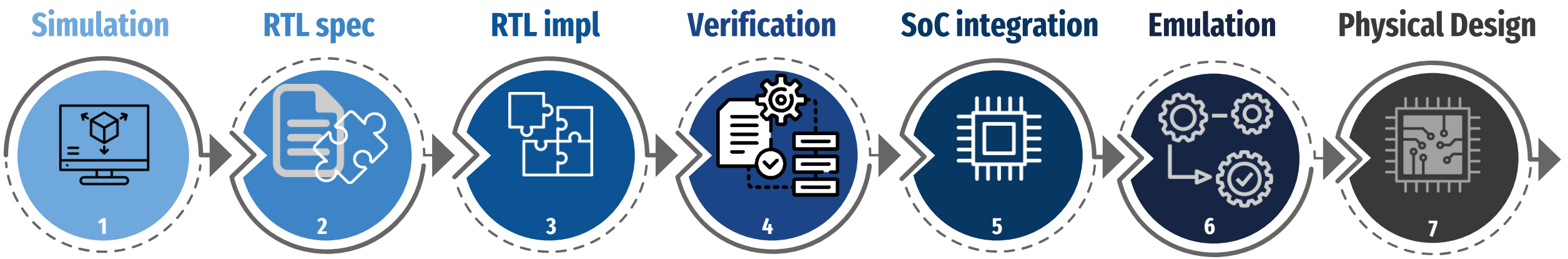
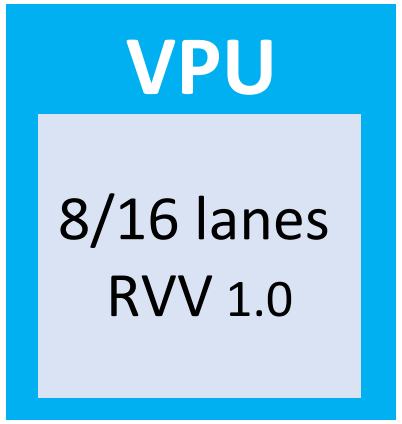
LOCA

RISC-V@BSC: Research



RISC-V@BSC: Innovation





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Sargantana *and more in:*
https://github.com/bsc-loca

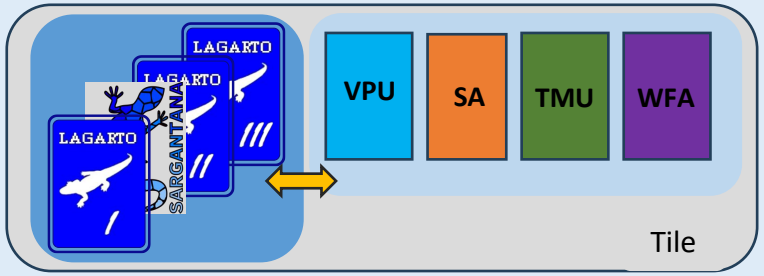
LOCA

RISC-V@BSC: Innovation

HPC Requirements
- High bandwidth
- Low latency
- Multiple memory controllers
- Larger caches and cache block sizes

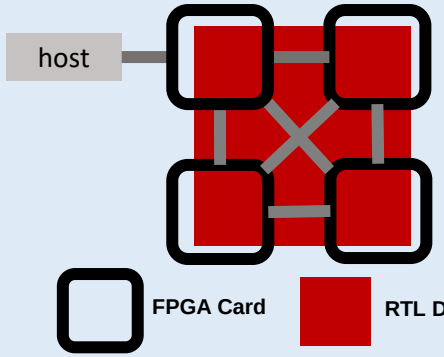
System level

Heterogeneous system

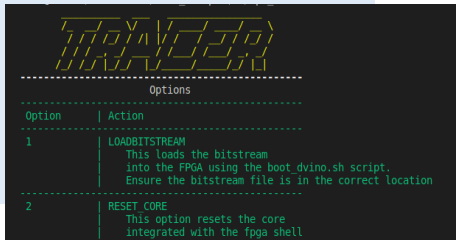


Compatible with

- Embedded FPGA Shell (U280, U55C, V80)
- Design partitioning



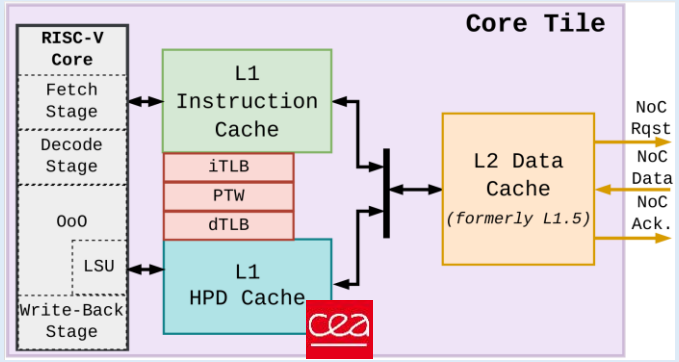
- FPGA RISC-V Tracer



Memory Hierarchy

Memory hierarchy:

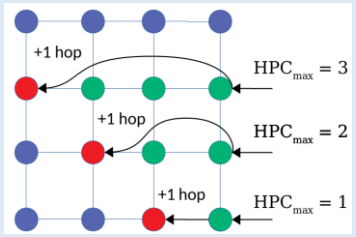
- 3-level cache hierarchy



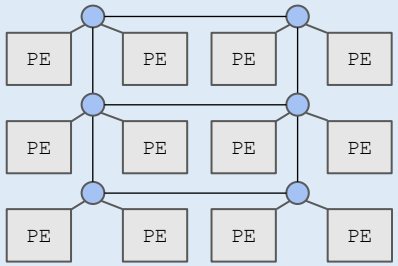
- Multi-memory controllers support (HBM)

ProNoC

- QoS, concentration, multi-hop bypass



Multi-hop bypass



Concentration = 2

U55C FPGA

LOCA

Lagarto RISC-V SoCs: tapeouts

Lagarto

- LHun 5-stage in-order
- 150MHz (external)
- **TSMC 65nm**
- 2.5mm2

DVINO

- LHun in-order
- Vector Pprocesing Unit
- PLL 600 MHz
- SDRAM mem cont
- HyperRAM
- **TSMC 65nm**
- 8mm2

Sargantana

- Sargantana 7-stage in-order
- PLL 1.2 GHz
- Custom extensions
- SDRAM
- **GF 22nm**
- Area: 2.9mm2

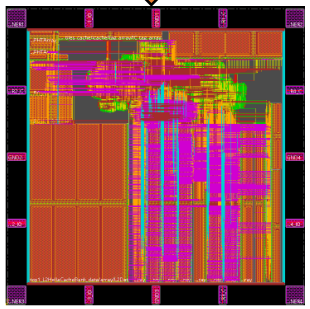
Kamaleon

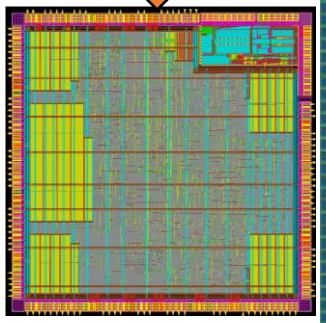
- Lagarto Ka 11-stage OoO
- PLL 1.2 GHz
- Accelerators:
  - Automotive
  - PQC
  - Genomic
  - PICOS
- **GF 22nm**
- Area: 9mm2

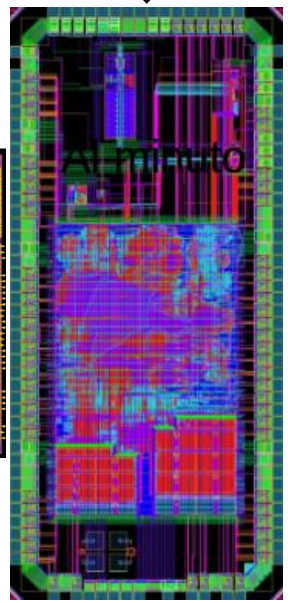
Multicore

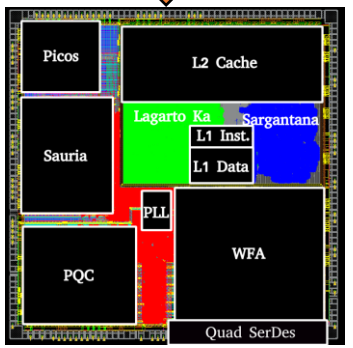
- Multicore:
  - Sargantana
  - LKa + VPU
  - LOx
- PLL 1 GHz
- NoC: OpenPiton
- Advanced technology node

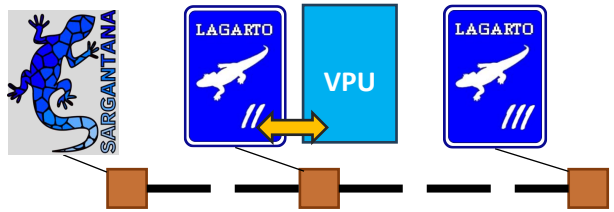
2019 | 2020 | 2021 | 2022 | 2023 | 2024











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RISC-V@BSC: Combining top/down & bottom/up approach

NEMO

Alya

PhysiBoss

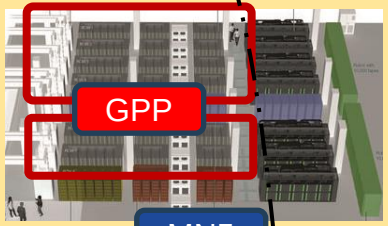
Phase 0 | Phase 1 | Phase 2 | Phase 3

Top-down

Learning from experience

MN4

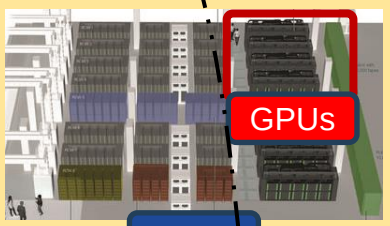
Next (current) Gen



MN5

Moving faster

Acc partition



MN5

Moving foward

MNx?

Bottom-up

European Processor Initiative

epi

VPU

BZL BARCELONA ZETTASCALE LAB

Multi-core

THE EUPILOT

DARE

SDV

Domain-specific acc

RISC-V Acc

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Thank you!!

Q&A

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