RISC-V asymmetric Linux RTOS multiprocessing

Eero Nurkkala, Janne Rosberg, Levente Tamas, Antti Takaluoma

An abstract super-scalable safe application platform

Integrated workstation-embedded software development

Modern configurable RISC-V platforms offer methods to create application optimized processing solutions. Processor cores may be assigned and customized to specific purposes. Customized cores may offer encapsulation of critical aspects, such as: security, safety, integrity, low-power, real-time processing and execution of general purpose (3rd party) computing applications.

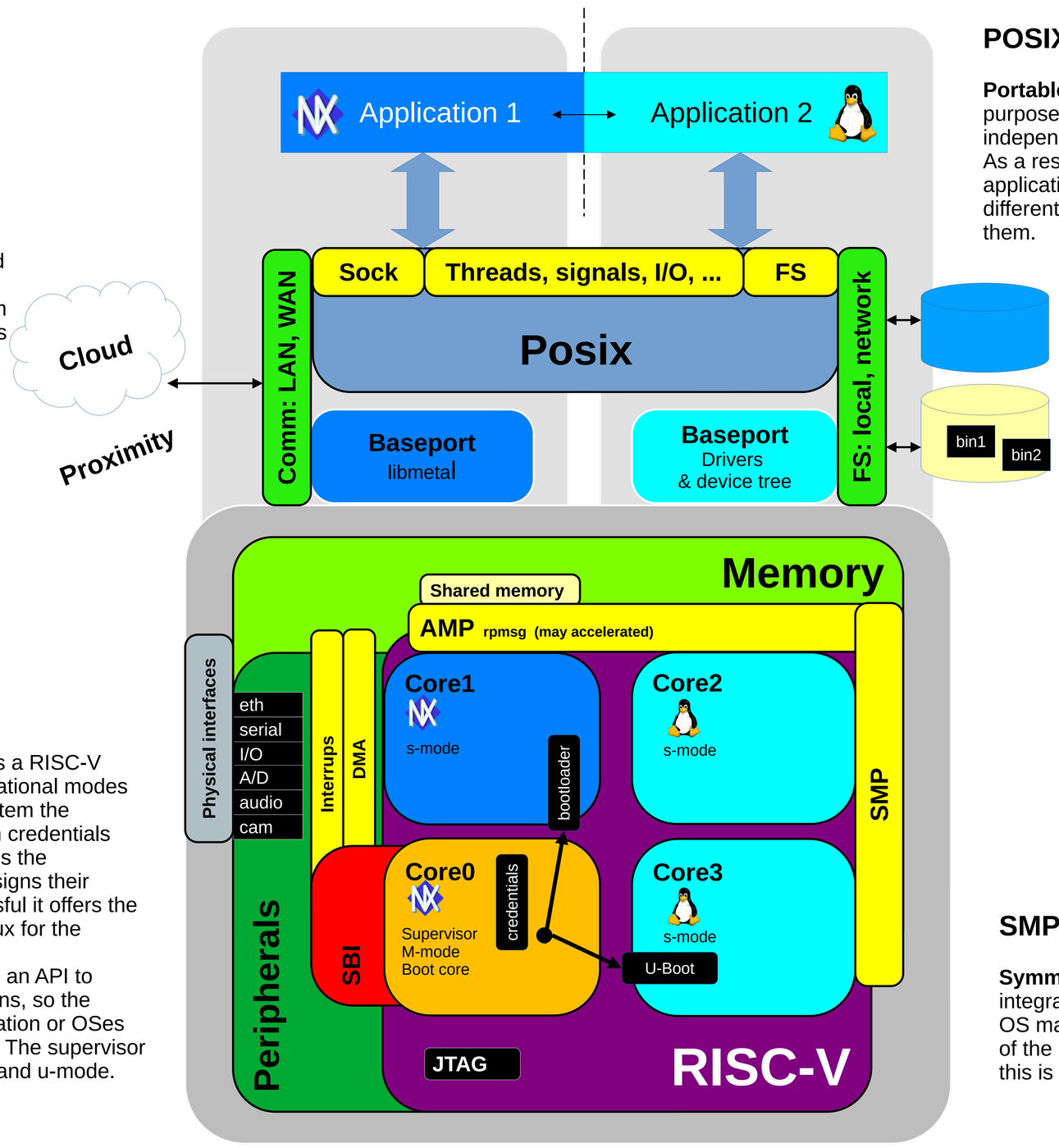
Introducing security, safety and low-power operations to “standard” computing platforms such as workstations and embedded Linux boards (e.g. Raspberry) is challenging. There exist special tweaks for the OS e.g. for real-time (RTLinux), but introduction of additional functions such as low-power and security increases complexity and the results is far from optimal. Due these changes, OS is being separated from original development branch and future maintenance becomes an issue.

The solution presented here encapsulates system security and integrity into one isolated (RTOS) core, real-time and low-power functions utilize another (RTOS) core(s) and for the general purpose “workstation-style” computing there is are a set of (Linux) cores. The security core keeps system credentials and supervises the software and system integrity.
As a second level, the RTOSes perform real-time and low-power functions. Finally Linux cores coordinate security, real-time and low-power functions and execute application software.
Integrating all these functions to cores of one processor offers potentially huge benefits on security, energy consumption, cost and scalability. Using unaltered OSes maintenance is simpler and there is less security risks in the future.

This type RISC-V AMP, SMP system may be optimized even further. Due to POSIX compatibility, both Linux and Nuttx applications may be executed in both systems. The binaries may be common and applications may be moved between domains (even at runtime).

Nuttx RTOS

Nuttx is a free open-source Real-Time Operating System (RTOS). Due to Portable Operating System Interface (POSIX) APIs, Nuttx is highly Linux compatible from the software point of view. Typically, applications may compiled directly to both systems, if required resources are available. Nuttx scales from 8-bit to 64-bit system and there exist ports to various platforms.
Nuttx supports c/c++, rust, zig, etc..
Originally (2007) released under a BSD license, it has been moved under the Apache-license.



POSIX

Portable Operating System Interface (POSIX) API’s purpose is to make the application software independent of the underlying hardware and OS.
As a result, it simplifies the software development, applications may communicate seamlessly between different OS-domains and also may move between them.

AMP

Asymmetric multiprocessing (AMP) means that the cores of the processor are not treated equally. In this context we assign some of the cores to Nuttx RTOS(es) and some to Linux. Linux utilizes SMP for the cores it has been allocated. Remote Processor Messaging (RMPsg) is used for communication between the different domains -- Nuttx and Linux. Linux has native support for RMPsg and now also Nuttx. By RMPsg data exchange between domains becomes simple.
AMP is started up by the supervisor (boot) core of the system using the SBI features of the RISC-V.
RPMsg may be implemented by software, but an implementation in special (accelerator) hardware will improve performance and lower energy consumption.

Supervisor core and SBI

Supervisor Binary Interface (SBI) is a RISC-V interface for accessing different operational modes of the RISC-V processor. On this system the assigned supervisor core has system credentials and secure boot. On boot up it verifies the bootloaders and Nuttx and Linux, assigns their peripherals and memories. If successful it offers the bootloader to Nuttx and uBoot to Linux for the startup.
At run time the supervisor core offers an API to encryption and authentication functions, so the possible security issues in the application or OSes won’t compromise the whole system. The supervisor core utilizes m-mode, OSes s-mode and u-mode.

SMP

Symmetrical multiprocessing (SMP) is an integrated feature of Linux. When enabled the Linux OS may assigns parallel tasks to to different cores of the processor. From an application point of view this is transparent.

Highly integrated super-scalable secure computing platform

Software development with FPGA for an optimized ASIC

Modern RISC-V designs are introducing new ways to create application optimized SOCs.
By integrating customized hardware accelerators the application’s performance is improved significantly, while the energy consumption goes down.

Open RISC-V implementations have enabled a new developer community. This community produces open solutions of processor features, peripherals, accelerators, development tools, etc..
By integrating well-tested solutions onto FPGAs, the learning curve is minimized, making it more straightforward to create application-specific optimized SOCs. The resulting developments could eventually transition into ASICs, influencing pricing, energy consumption, and performance while introducing disruptive products.

Application optimized custom SOCs significantly improve product size, cost and MIPS/W

PULP
Parallel Ultra Low Power

Open **Parallel Ultra-Low-Power Processing-Platform** (PULP) is a RISC-V based open source processor implementation. It has various 32-bit and 64-bit single- and multi-core variants with a rich set of peripheral options. By utilizing FPGA-based boards, system development can ramp-up easily.
PULP is developed by the Integrated Systems Laboratory of the ETH Zürich

This work is based on the studies of the Fractal project 2020-2023

Funded by the European Union

Offcode Oy is an engineering office for the extreme SW/HW applications

www.offcode.fi

OFFCODE