Hippomenes: An Experimental Implementation of the RISC-V RT Real-Time Extension

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Abstract

In this work we propose the RISC-V RT (Real-Time) extension with notable outstanding features:

- Nested Core-Local Interrupt Controller bringing interrupt latency and execution overhead to zero,
- hardware assisted zero jitter, cycle accurate time-stamping, with the addition of
- atomic read/write peripheral access through CSR mapping, and
- Real-Time Monitoring and Trace bringing zero overhead hardware event monitoring and constant-time tracing.

We present Hippomenes as a synthesizable/executable specification for the proposed RISC-V RT real-time extension. Lastly, we introduce Rust and RTIC based software tooling, with the formal model underpinning ensuring safety and security of the system by construction

1 Introduction

The Core-Local Interrupt Controller(CLIC) proposal introduces an interrupt controller aimed at embedded systems. However, the software-centric approach to context switching introducing latency and overhead detrimental to desired scheduling properties.
The introduced overhead has been addressed in multiple previous works, most notably by Mao et. al.[4] and Balas et. al.[1], however, none of the solutions manage to outperform the state-of-the-art in a hard real-time (worst-case) context.

Processor	ISA	Interrupt Latency	Nesting
Arm Cortex M4	ARMv7-M Thumb	12	Hw
ESP32-C3[3]	RISC-V	48	Sw
CLIC[2]	RISC-V	33[a]	Sw
Mao et. al.[4]	RISC-V	13	Hw
Balas et. al.[1]	RISC-V	6[b]	Hw/Sw
This work (RISC-V RT)	RISC-V	0	Hw

Figure: Interrupt dispatch latencies of select microcontrollers.

[a] SW-based solution, presuming the best-case of single-cycle instructions, and optimal traps. [b] Not applicable to worst-case scenario.

2 RISC-V RT

RISC-V RT consists of a set of optional extensions targeting the hard real-time domain.

2.1 NCLIC

The Nested CLIC (NCLIC) is a novel interrupt architecture, extending on the current CLIC with a stacked register file and a CSR-based interface allowing 0 interrupt latency and predictable timing behavior by circumventing potential bus arbitration.

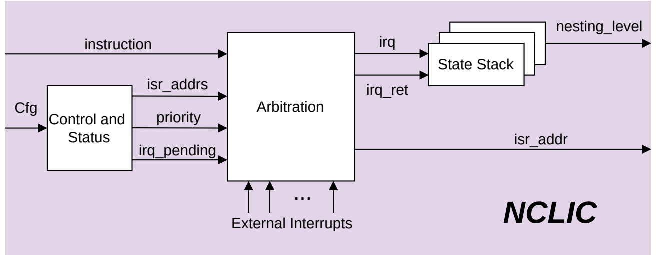

Figure: Structure of the NCLIC interrupt controller.

2.2 RTMT

Real-Time Monitoring and Trace is an architecture extension providing zero-overhead, cycle-accurate monitoring and timestamping of hardware events. Transport leverages on preemptive framing using the real-time Nested COBS protocol.

3 Hippomenes

The Hippomenes architecture places the focus on predictable behaviour and performance in a hard real-time context, hence all instructions are guaranteed to execute in a single cycle. The simplicity allows using Hippomenes as a basis for rapid prototyping and synthesizeable specifications of proposed extensions.

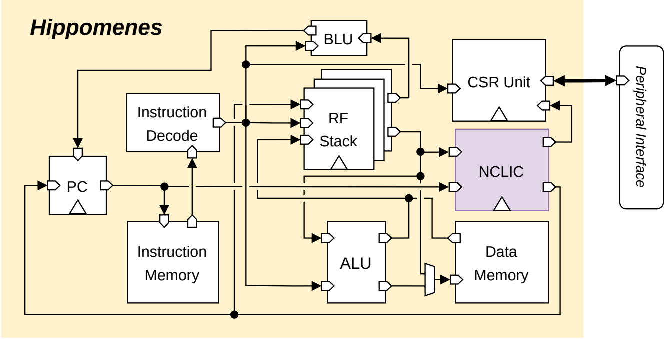

Figure: The top-level architecture of Hippomenes.

4 Rust+RTIC

The Rust-based RTIC framework allows the programmer to define an executable Stack-Resource Policy model. This formal underpinning guarantees deadlock freedom and bounded priority inversion. RTIC maps each task to an interrupt handler, leveraging on the interrupt controller for scheduling acceleration.

Task	Priority	Resources
Timer	2	{r}
High	3	
Low	1	{r}

Event	Timestamp
Timer entry	54
High entry	56
High exit	57
Timer exit	58
Low entry	59
r lock	61
r unlock	63
Low exit	64

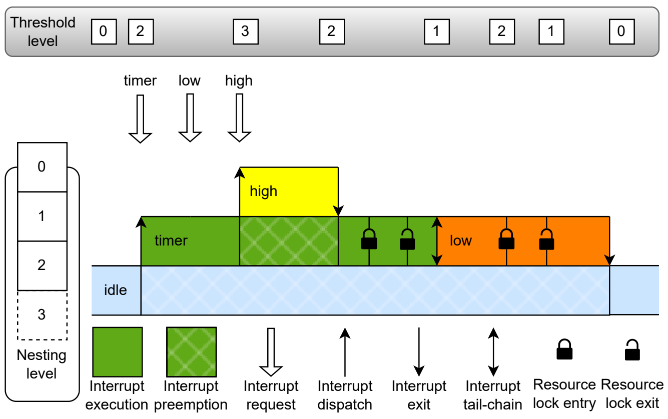

Figure: Task-resource mapping and execution diagram of a simple RTIC application. The captured RTMT event timestamps confirm the zero-latency nature of Hippomenes.

References

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