

Andrew Johnston, Senior Functional Safety Manager [andrew.johnston@imgtec.com](mailto:andrew.johnston@imgtec.com)  
 Dr. Varadan Veeravalli, Principal Functional Safety Engineer [varadan.veeravalli@imgtec.com](mailto:varadan.veeravalli@imgtec.com)  
 Kenneth Rovers, Senior Principal Hardware Architect [kenneth.rovers@imgtec.com](mailto:kenneth.rovers@imgtec.com)

## DID YOU KNOW?

Imagination Technologies have been pioneering GPU design and technology for over **30 years**, and since 2019 have been incorporating **RISC-V CPUs** in our **PowerVR GPU** products. This includes independently certified **ISO 26262 ASIL-B GPUs** from 2021 onwards.

## GPU ARCHITECTURE EVOLUTION



ASIL-D Systematic Development Process Certified

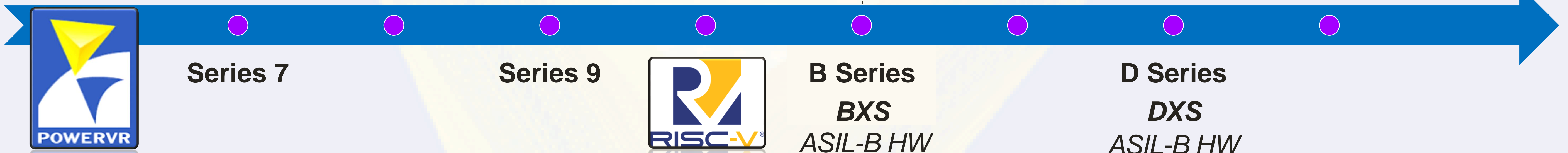
Since 1995...

Series 8

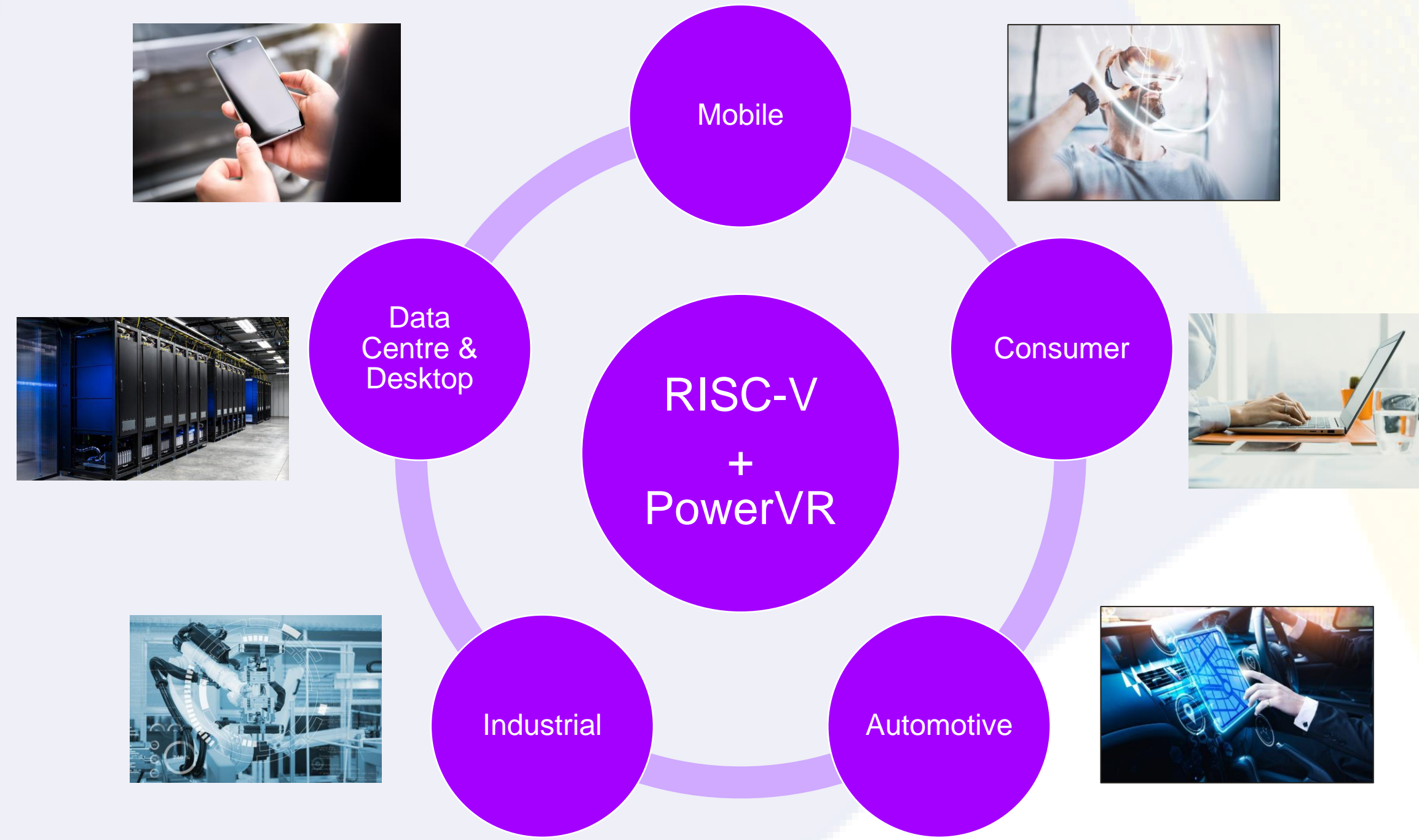
A series

C Series

...Future



## FLEXIBLE & SCALABLE IP

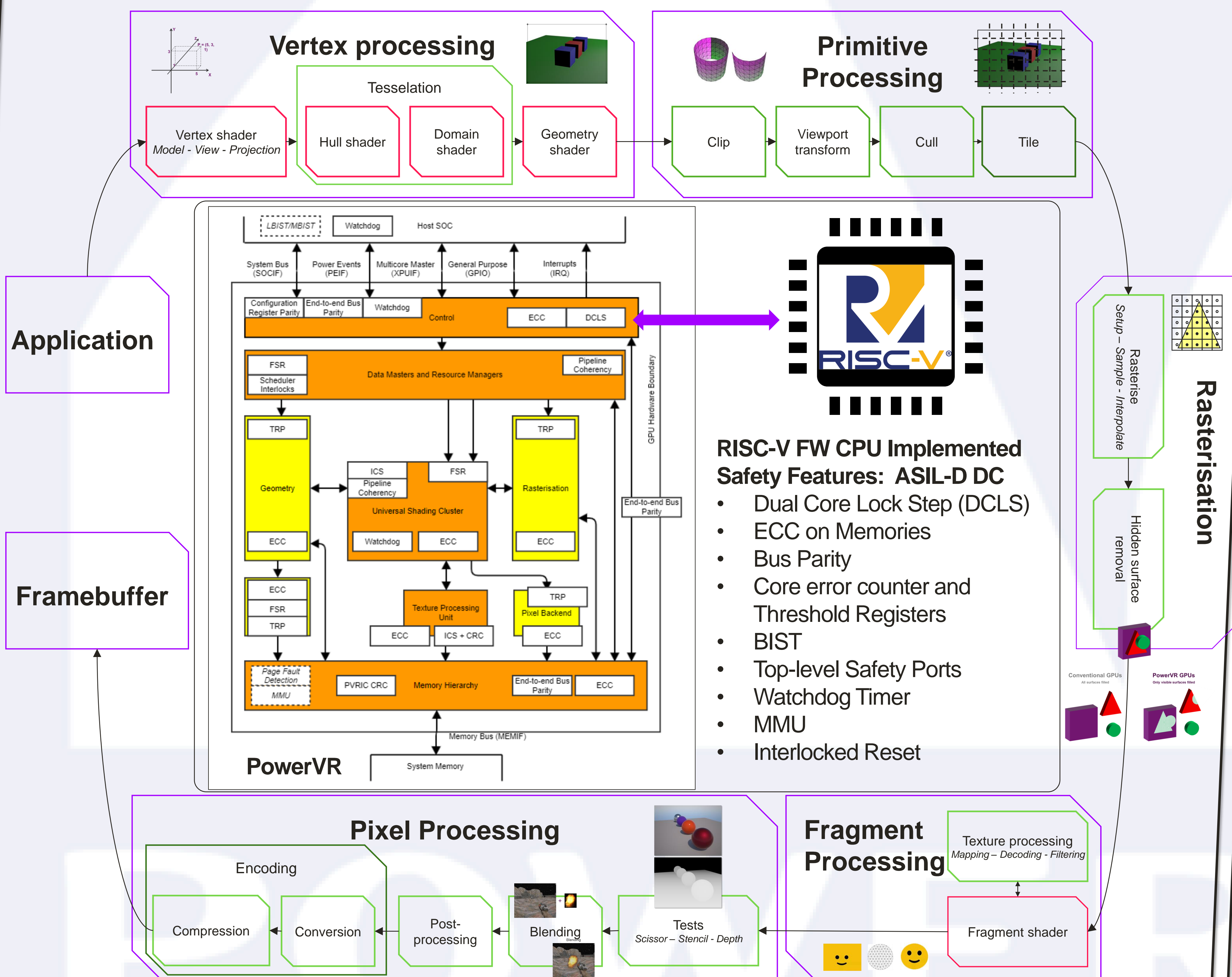


## THE CHALLENGE...

- Power is nothing without Control
- PPA improvements on every generation
- Need high performance area-efficient silicon
- Need to support tomorrow's complex compute intensive use-cases today
- Need both Flexibility and Scalability
- Need Secure, Safe and Reliable IP

- Functional Safety
- Efficiency
- Performance
- Scalable

## GRAPHICS PIPELINE & DXS GPU SAFETY ARCHITECTURE



## GPU BENEFITS

- RISC-V:**
- Clean, simple, compact
  - High Performance
  - Easy to integrate



**BXS & DXS GPU: ISO 26262 ASIL-B HW architectural metrics achieved:**

- Independently certified Safety Management Process: ASIL-D Systematic Process and tools
- **Distributed Safety Mechanisms**
- **Defence-in-Depth** approach, each major subsystem has more than one safety mechanism; **Graceful Degradation**
- **Embedded ASIL-D compliant RISC-V CPU**
- Performance, Power, Area (PPA) and Safety objectives achieved

- Supported by our advanced **Catapult** range of RISC-V CPU IP:
- **RTXM-2200** (32 Bit)
  - **APXM-6600** (64 Bit)

**Result: Low power consumption, high performance, Safe embedded IP cores**

ASIL-B Distributed Safety with Defence-in-Depth Safety Mechanisms, Controlled by an ASIL-D compliant RISC-V CPU