

Basilisk: Achieving Competitive Performance with Open EDA Tools on an Open-Source Linux-Capable RISC-V SoC

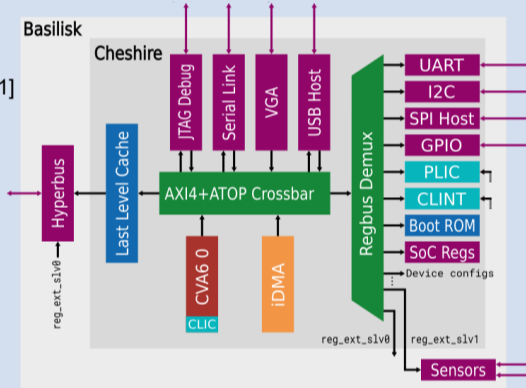
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1 Introduction and Motivation

- OS EDA flow profits multiple communities
 - Academia:** NDA-free and open collaboration
 - Education:** Limit-free understanding of the EDA tools
 - Industry:** Transparent chain-of-trust, more skilled personal
- OS EDA flows exist, achieving **good** results for **small** designs
 - Flows and tools show cracks with multi-million-gate designs
 - No **end-to-end open** Linux-capable SoC yet

Basilisk SoC

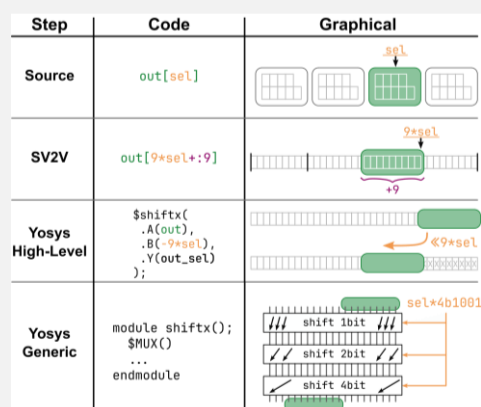
- Cheshire SoC platform^[1]
- Linux-capable
- CVA6 64-bit RISC-V
- USB 1.1 host
- VGA display
- External, digital-only DRAM interface



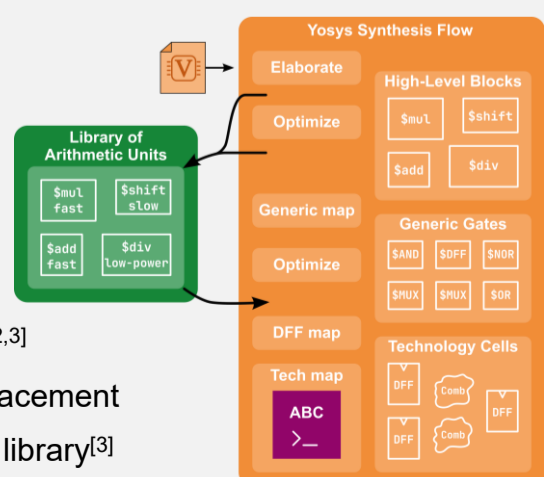
- Implement Basilisk **end-to-end open** (Yosys, OpenROAD)
 - Improving OS EDA tools and flow** along the journey
 - Realistic benchmark** for OS EDA tools to grow

2 Synthesis Improvements

- Part-select operation in Yosys
 - Prior to v0.34: barrel **shifter**
 - More complex than mux
 - High-cost** gate-level netlist
 - Contributed** fix in v0.36
 - Opt. pass** inferring MUX
 - 1.5x in area, 2.9x in RAM**

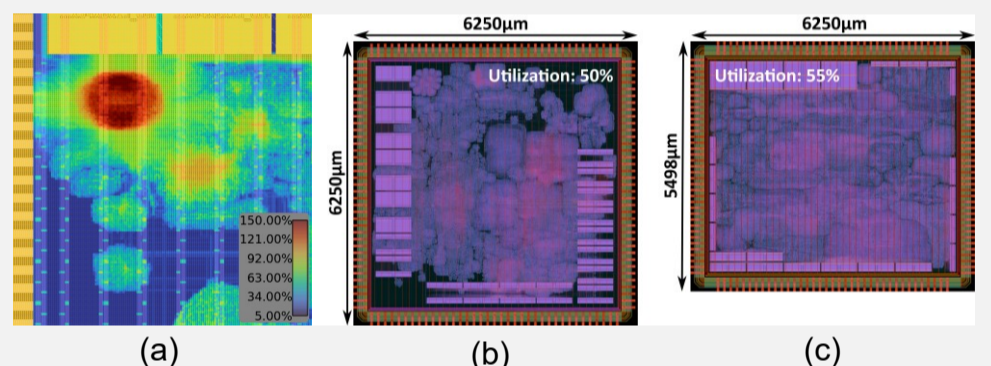


- ABC: optimized scripts
 - Lazy man's synthesis**
 - Cheaper** optimization run **multiple** times
 - 2.3x in timing**
- Library of arithmetic units^[2,3]
 - Arithmetic operator replacement
 - Optimized open-source library^[3]



3 Place & Route Improvements

- Focus on OpenROAD's flow scripts
 - Improved **sequence** of commands
 - Hyperparameter tuning to **reduce density hotspots**
 - Density force:** push cells to achieve target density
 - Wire force:** attract connected cells to reduce wire length



- (a) example of **over 100%** density at the site of the **bootrom**
- Untuned (b) and tuned (a) hyperparameters
- Our flow results in more uniform density **without hotspots**

4 Results and Conclusion

- Improve flow:
 - 1.6x** in area
 - 2.3x** in timing

	Yosys-0.33	MUX	ABC	LAU
Logic area	1.8 MGE	1.4 MGE	1.1 MGE	1.1 MGE
Timing	33 MHz	37 MHz	71 MHz	77 MHz
Logic levels ^a	182 LL	149 LL	54 LL	51 LL
Runtime ^b	5.4 h	2.8 h	2.2 h	2.2 h
Peak RAM ^c	217 GB	105 GB	76 GB	75 GB

^a Number of logic gates in longest path ^b 2.5 GHz Xeon E5-2670

- Taped Basilisk in **May 2023**
 - First end-to-end open Linux-capable SoC**
- Room for improvement
 - Timing-driven** synthesis
 - Automatic** hyperparameter tuning



References

- Ottaviano et al., Cheshire: A Lightweight, Linux-Capable RISC-V Host Platform for Domain-Specific Accelerator Plug-In, IEEE TCAS-II, 2023
- VHDL Library of Arithmetic Units: https://iis-people.ee.ethz.ch/~zimmi/arith_lib.html
- Library of arithmetic units: <https://github.com/pulp-platform/ELAU>

