Explorative Surveying RISC-V Open Hardware and Specifications for Mixed-Critial Systems

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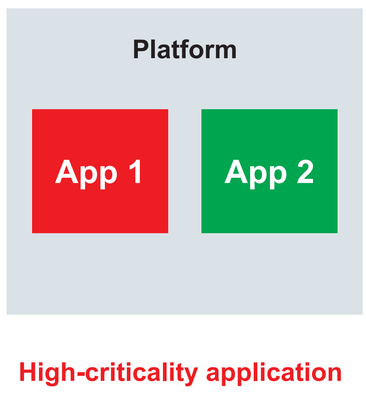
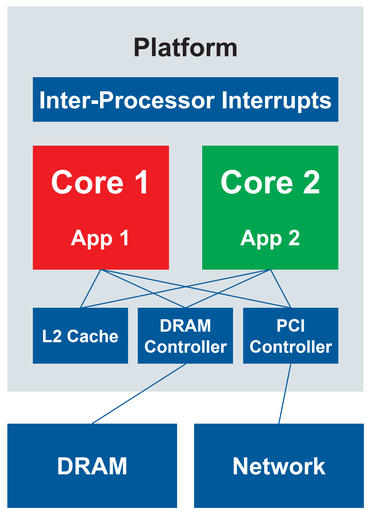
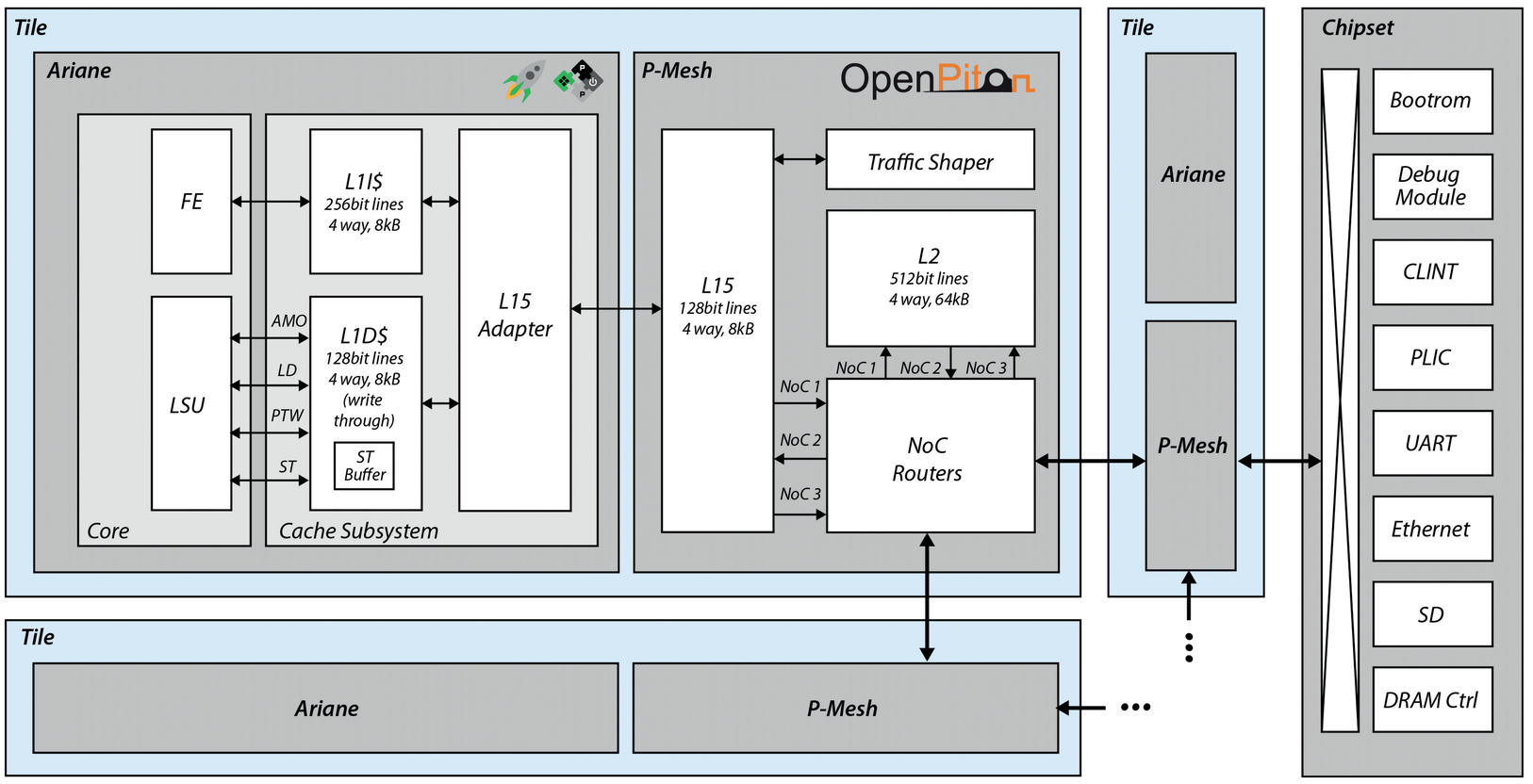
Mixed-critical systems are essential in modern computing, where applications of different criticality levels share the same hardware platform(s) and/or resources. This paper explores the robustness and implementation of mechanisms for such mixed-critical systems utilizing RISC-V specifications and available open hardware. In particular, the CVA6 processor and OpenPiton System on Chip (SoC) are used. We also research the mixed-criticality suitability of core-to-core communication, resource management, and specific components like performance counters, memory, and caches. Furthermore, we discuss future developments of mixed-critical systems utilizing open hardware.



- **Mixed-criticality systems:** Run applications with different criticality levels (often safety-focused) on the same HW platform.
- **Hardware separation:** Physically separate HW for critical applications (during design/planning).
- **Benefits of mixed-criticality systems:**
  - More flexible than physical separation.
  - Many applications in modern computerized systems.
- **Simplest case:** One critical and one less critical application on the same platform.



- **Traditional time-sharing systems:** Processes run concurrently on the same processor.
- **Modern approach (multi-core processors):** Cores are assigned to different applications.
- **Mixed critical systems:** Cores share resources (L2 caches, DRAM, PCI controller).
- **Configuration** ensures high-criticality applications aren‘t blocked by lower-criticality ones.



www.github.com/PrincetonUniversity/openpiton

- **RISC-V for mixed-critical systems:** Malleability of ecosystem easies development of dedicated mixed-criticality support. Also open HW components allow independent verification of safety / security properties.
- **Resource management:**
  - Performance counters help allocate resources.
  - Memory management offers isolation (MMU) but shared memory (DRAM) can cause issues. Cache partitioning (not yet standardized) can improve isolation.
- **Communication and synchronization:**
  - Mechanisms for strict isolation between domains (like multiple OSes) are under development.
  - Deterministic communication (essential for safety) remains a challenge.

- **Security:** Speculative execution poses security risks. „fence.t“ instruction (concept) could mitigate these risks.
- **OpenPiton SoC example:** HW / SW monitoring for systems with shared resources (common technique: partition some resources with hardware and manage others with OS-based on performance counters).
- **Future directions:** Specifying a more mixed-criticality-oriented SoC for future hardware development. Exploring reliability assessment techniques.

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