Towards Coverage Analysis for Translating Instruction Set Simulators

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Motivation
• VPs and ISSs are pivotal for early design verification and architecture exploration
• DSLs and modeling tools such as nML, Codaship and CoreDSL2 allow fast & easy definition of custom ASIPs
• Functional and formal verification is a crucial aspect of deploying new VPs and ISSs, and increases in complexity once model-based extensible ISAs are used
• Coverage analysis provides a good overview of how much input source is targeted by a given test suite
• Monolithic ISSs are easily tested for coverage with standard tools
• Modern ISSs utilizing DSL-based target ISA specification and dynamic binary translation cannot be analyzed by traditional tools

Goal: Derive and implement a coverage analysis methodology for DSL-based, DBT accelerated simulators

Application in a DBT ISS

Test Setup
Test Script
CoreDSL Desc.
SIM.
Config
Test Cases
CVA6 VP
Listener

Test Script
VP Config
Table 1 ISS Test Setup

• riscv-tests instruction-level test suite as basic initial plausibility check to show importance of coverage analysis
• Automated test script to simplify targeted, parallel execution

Test Cases
Selected Test
Figure 1 ISS Test Setup

• Additional comparison against OpenHwGroup CVA6 processor to check improved test cases

Case Study

LCOV - code coverage report

<table>
<thead>
<tr>
<th>Source code</th>
<th>Line data</th>
<th>Source code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Covergence Tracker</td>
<td>Cov. DB</td>
<td>Cov. Report</td>
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<td>Cov. Tracker</td>
<td>Arch. Model</td>
<td>JIT Code</td>
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<tr>
<td>CoreDSL Desc.</td>
<td>Code Generator</td>
<td>Coverage Analyzer</td>
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• Coverage tracking addition to existing DBT ISS ETISS
• ETISS is built on a CoreDSL2 model description, code generator toolchain M2-ISA-R parses model and generates architecture simulation model
• M2-ISA-R is extended to embed coverage tracking information into simulation model
• Analysis tool consolidates generated coverage data, matches against metadata from architecture model and outputs LCOV compatible report files

Figure 3 DBT ISS Coverage Analysis Dataflow

• Overall: 89.7% line coverage, 92.5% function coverage, 68.8% branch coverage for riscv-tests
• Critical coverage misses in shift instructions and rounding mode for floating-point instructions reveal bugs in CoreDSL2 and CVA6 cores
• Targeted fixes implemented for coverage misses possible
• Future Additions: Analysis of edge cases, register usage, automatic test case generation and extension, performance improvements (~75 MIPS default vs 2.5 with coverage analysis active)

Figure 4 riscv-tests Integer Instructions Coverage Example

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Open Source: https://github.com/tum-ei-eda

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