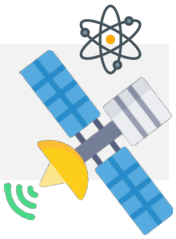
Selecting **different RISC-V ISA extensions** for compiling **impacts** on **soft error sensitivity**

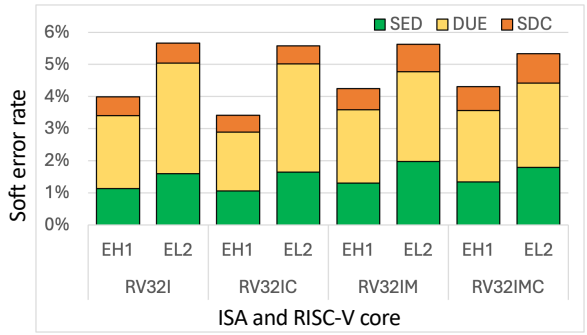
Comparison of sensitivity to soft errors, depending on ISA extensions, for RISC-V cores VeeR EH1 and EL2 from Western Digital

- **Space Radiation** may produce soft errors
- **+60% of +8.000 satellites** in the last 3 years
- **RISC-V** coming to **space applications**
- **Commercial CPUs** for non-critical tasks

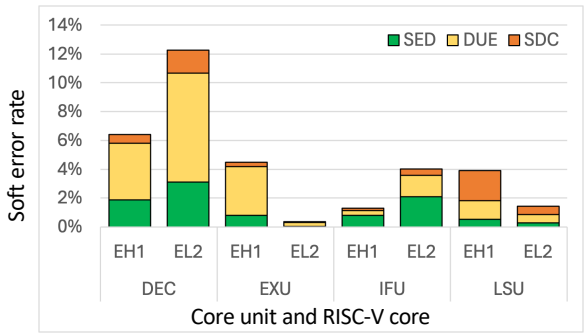


May ISA compiling-target selection improve radiation resilience?

Result 1: Error rate in EH1 and EL2 when C code is compiled for different ISA targets.



Result 2: Soft error rate by core unit. The **DEC** unit is the **most sensitive** for both processors.

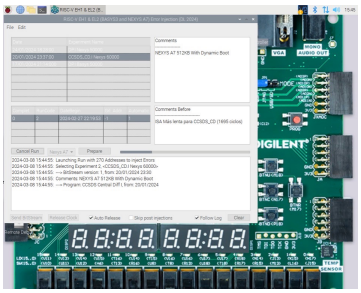


SED: Single Event Delay – DUE: Detected Unrecoverably Error – SDC: Silent Data Corruption

Experiment

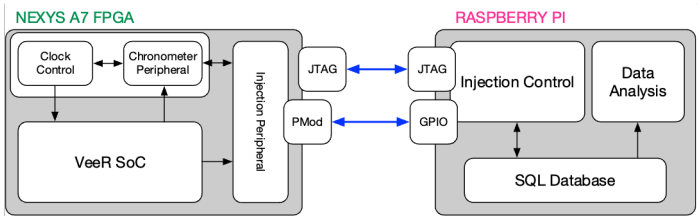
20 campaigns | 300.000 injections | Microarchitecture Registers | 99% C.L. 1% error

SETUP RTL simulation - Baremetal C code



INJECT

- Non-intrusive
- Based on partial reconfiguration
- 5 injections per second



Conditions: These findings apply to Veer EH1 and EL2 RISC-V processor cores using three baremetal C programs: SHA256, Dot product and CSSDS 123.0-B-2 Hyperspectral compression algorithm.

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