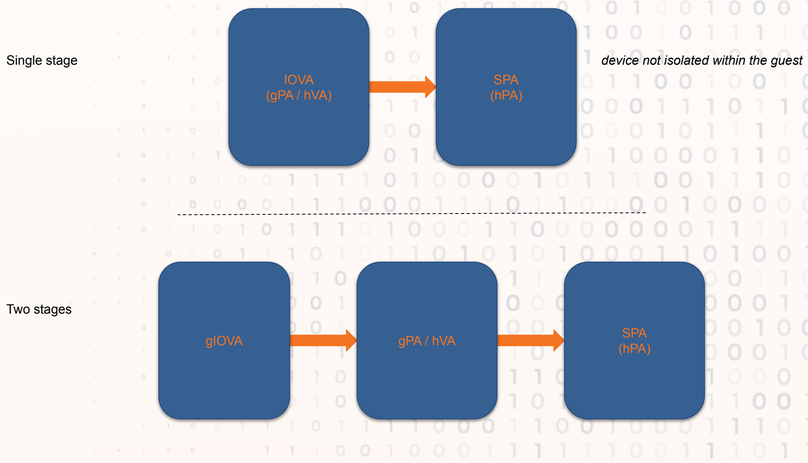
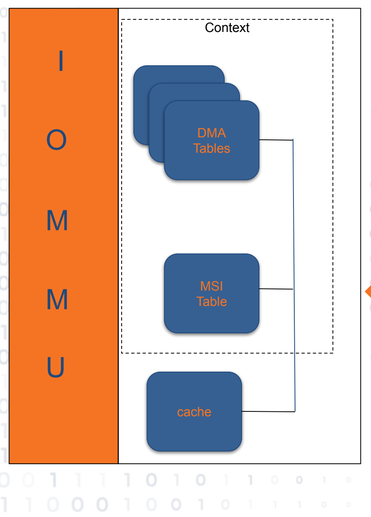
Device Assignment with the RISC-V IOMMU

RISC-V IOMMU Translation

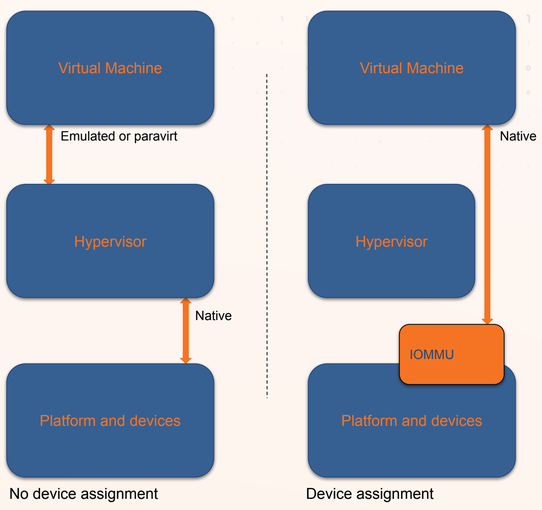


RISC-V IOMMU Page Tables

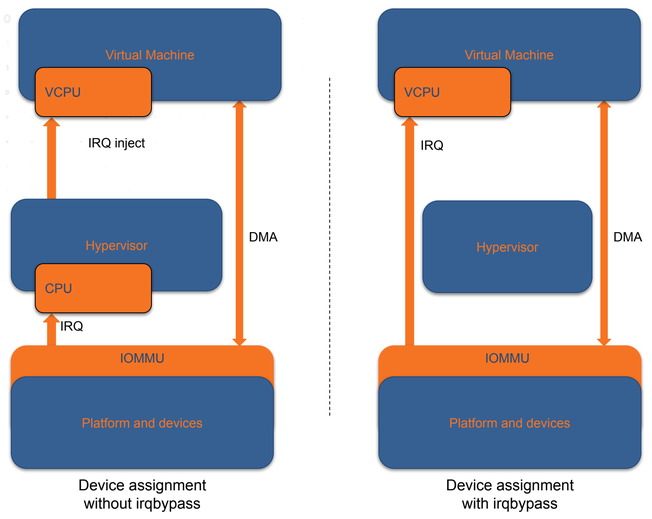


The hypervisor can modify the MSI table independently of subsystems which only modify the DMA tables. (MSI PTEs have a special format.)

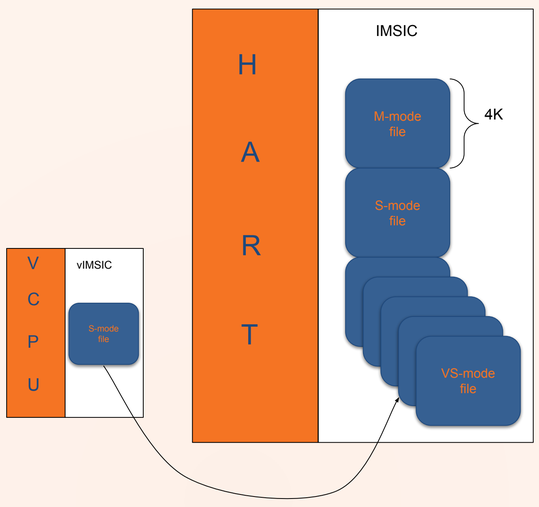
Device Assignment



irqbypass

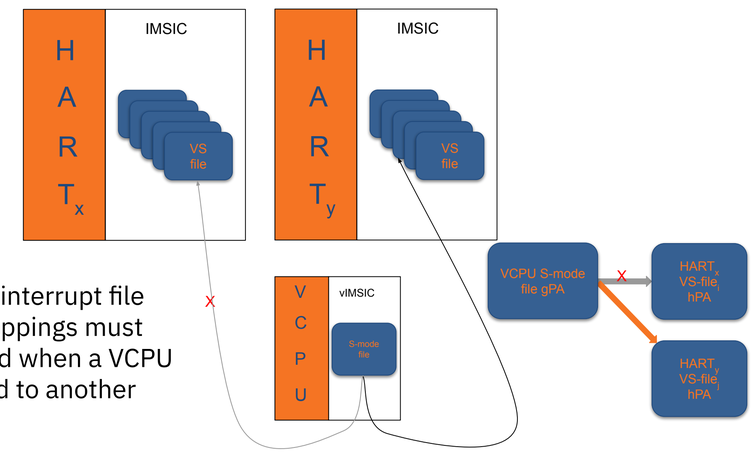


RISC-V AIA IMSIC VS-mode files



- The maximum number of VS-mode files is 31 for RV32 and 63 for RV64.
  - The server-soc specification currently requires 5.

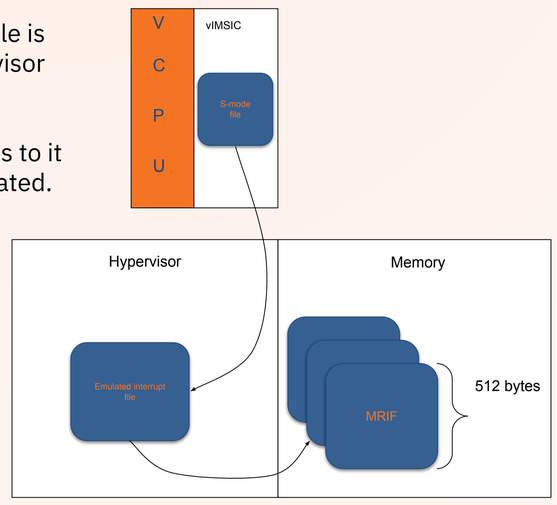
VCPU Migration with VS-mode files



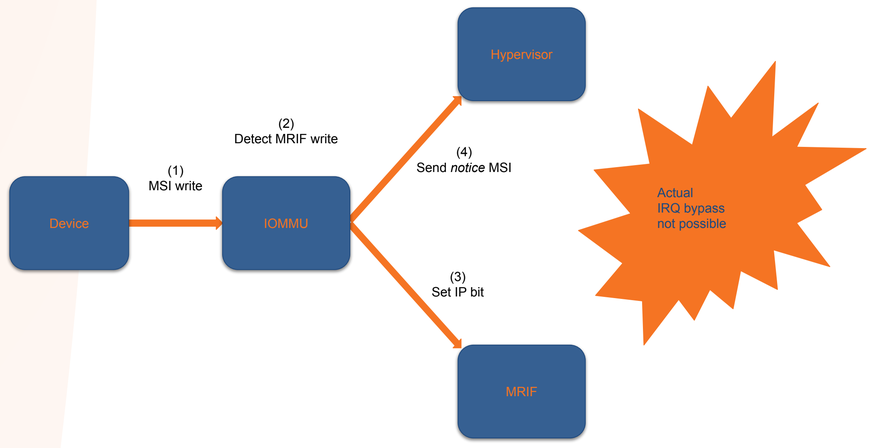
- The guest interrupt file and its mappings must be updated when a VCPU is migrated to another hart.

RISC-V AIA IMSIC MRIFs

- When no VS-mode file is available, the hypervisor provides an MRIF (*memory-resident interrupt file*). Access to it is trapped and emulated.



VCPU Migration with MRIFs



VENTANA MICRO