Next-Gen TETRISC SoC - A Quad-Heterogeneous Design for Adaptive Fault Tolerance

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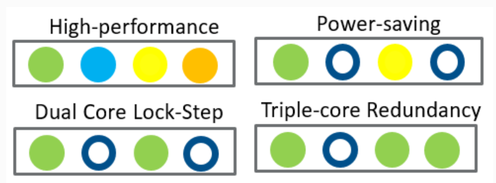
MOTIVATION

- Increasing demand for real-time data processing in reliability-critical applications, such as aviation and aerospace.
- Overcoming limitations of traditional static fault mitigation methods.
- Requirements for real-time reliability monitoring networks.
- Addressing the dynamic reliability needs of systems to ensure optimal operation under normal and severe conditions.

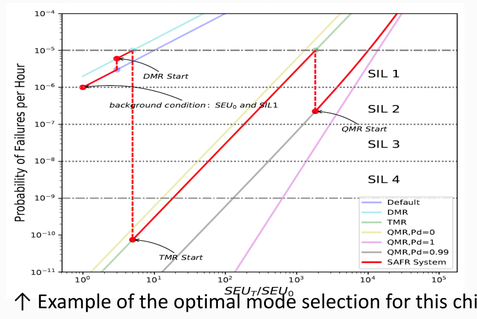
GOALS

- Develop an adaptable and resilient system for reliability-critical applications.
- Enable on-demand reconfigurable redundant system allocations under harsh conditions.
- Implement an on-board monitor network for enhanced system monitoring.
- Realize real-time dynamic tradeoffs between system reliability, power consumption and performance.

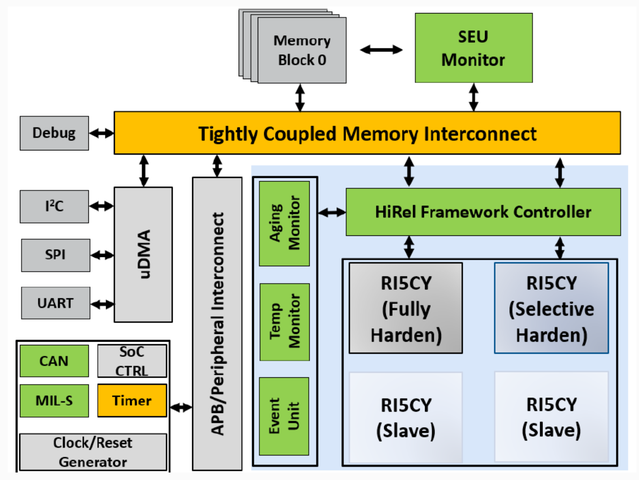
Next-Gen TETRISC SoC Overview



↑ Operating mode groups for the quad-core multiprocessing system.



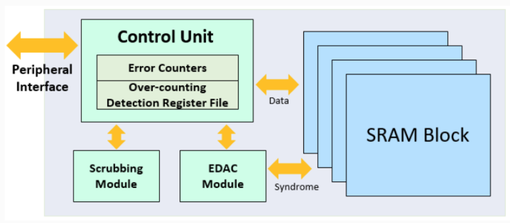
↑ Example of the optimal mode selection for this chip.



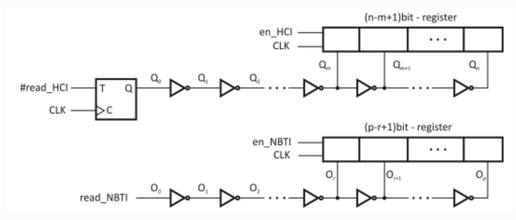
↑ The system architecture of the new TETRISC SoC.

- Reconfigurable quad-core SoC based on the open-source single-core microcontroller architecture PULPissimo, utilizing the RISC-V instruction set.
- Four heterogeneous RISC-V RI5CY cores: fully hardened, selectively hardened, and two unhardened cores with multi-operation modes
- Integration of multiple on-chip monitors for SEU (radiation), core aging, and temperature monitoring.
- Dynamic tradeoffs between reliability, performance, and power consumption.
- Intelligent HiRel framework controller for hybrid critical edge computing applications.
- Three operating mode groups: high performance, power saving, and fault tolerance.
- Task synchronization between different cores can be achieved in two clock cycles.
- Will fabricated with 130nm IHP technology.
- Radiation testing planned for the target ASIC design

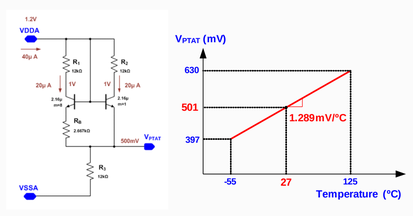
On-chip Reliability Monitor Network



↑ On-chip SRAM-based Single Event Upset Monitor [1].

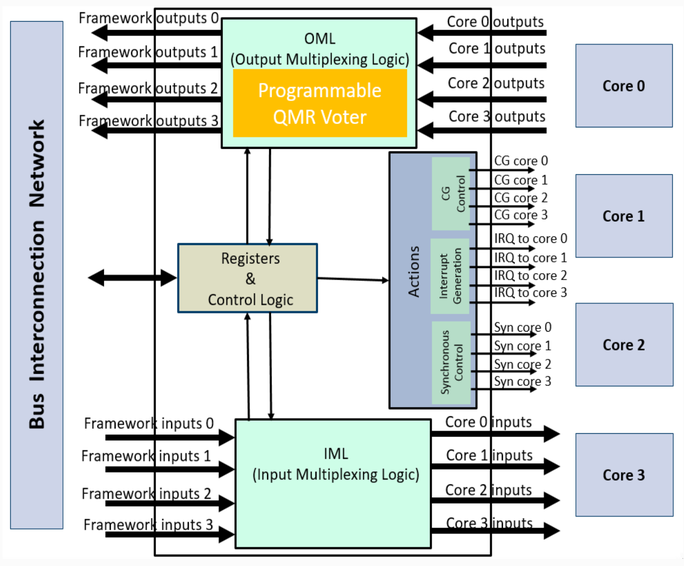


↑ HCI & NBTI Aging Monitor [3].



↑ Temperature Monitor.

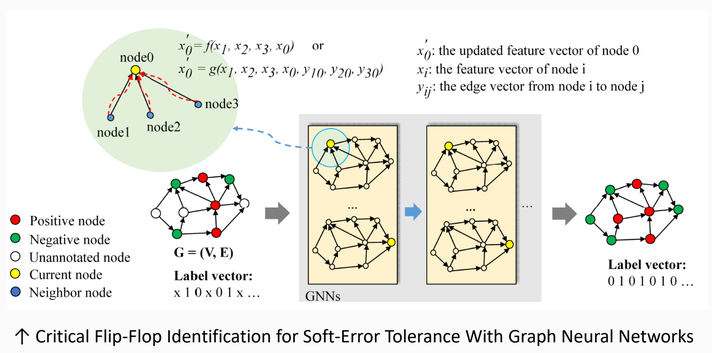
- A variety of existing on-chip reliability monitors can be effectively integrated into the agile development flow.
- Aging monitors to continuously track the status of critical paths.
- Analog & digital temperature monitors for precise on-chip real-time tem status monitoring.



↑ Block diagram of the HiRel Framework Controller.

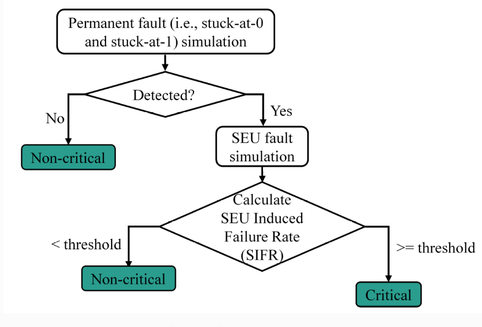
- A dedicated fault management system to record and manage faults, bolstering system reliability and facilitating efficient troubleshooting
- Manages all core inputs and outputs, implementing various operation modes with core-level N-Modular Redundancy (NMR) and clock gating.
- Includes a binary matrix-based programmable NMR majority voter that provides dynamic selection.

GNN-Based Selective Harden & Fault Simulation Prediction

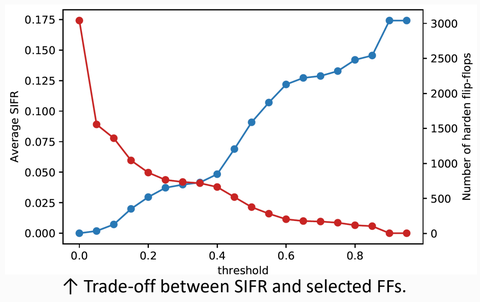


↑ Critical Flip-Flop Identification for Soft-Error Tolerance With Graph Neural Networks

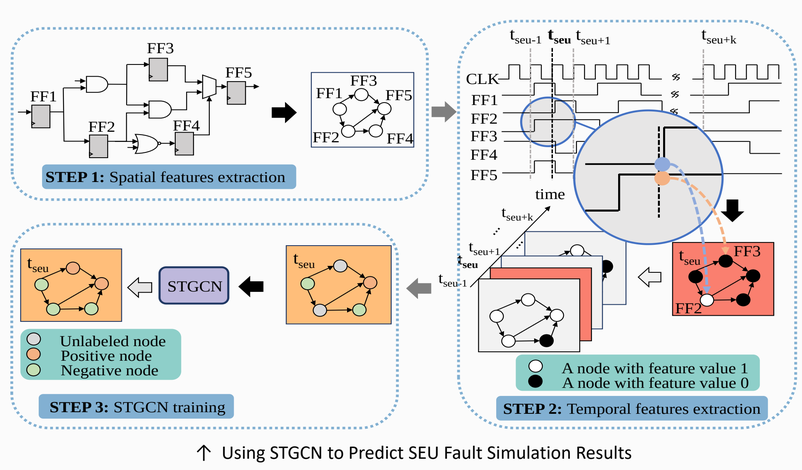
- The Graph Neural Network (GNN) model is represented by three matrices or tensors following.
  - Feature matrix: represent the features of each flip-flop;
  - Adjacency matrix: represent the connections of flip-flops;
  - Edge tensor: represent the feature of edges between FFs
- SEU Induced Failure Rate (SIFR) of a flip-flop is defined as the likelihood of SEU faults propagating to observation points. It is calculated based on fault simulation results.



↑ Fault injection flow of the critical FFs selection



↑ Trade-off between SIFR and selected FFs.



↑ Using STGCN to Predict SEU Fault Simulation Results

- Objective: Accelerate SEU fault simulation using Spatio-temporal Graph Convolutional Networks (STGCN).
- Results: The approach achieves over 95% accuracy, significantly reducing simulation time by up to 60%.

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