



### **CVA6-PLATFORM**

VENDOR-NEUTRAL, CYCLE-ACCURATE, CLOUD-BASED RISC-V SW DEVELOPMENT

Authors

Presenters

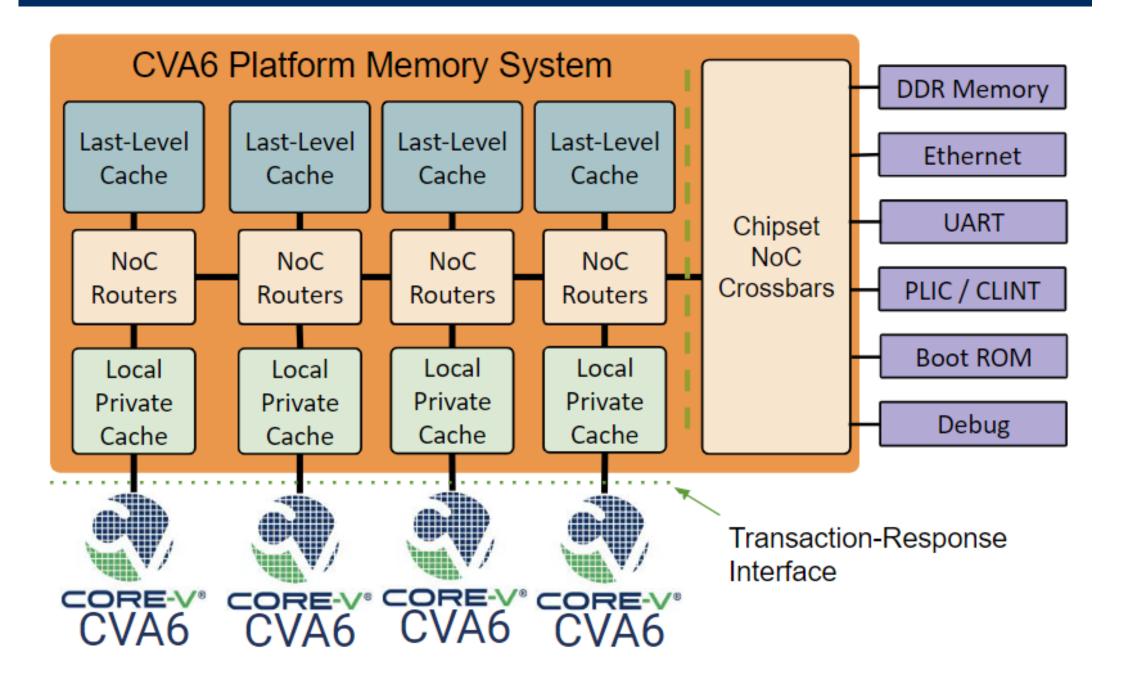
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# **CLOUD-BASED CVA6 S/W DEVELOPMENT**



# **USE CASE SUMMARY**

CVA6-Platform is designed to support software development for

- Firmware
- Kernel
- Applications

#### Configurations include

- Locally hosted FPGA development board
- Cloud-hosted, scalable FPGA resource
- Cloud-hosted, scalable FPGA resource with full CI architecture

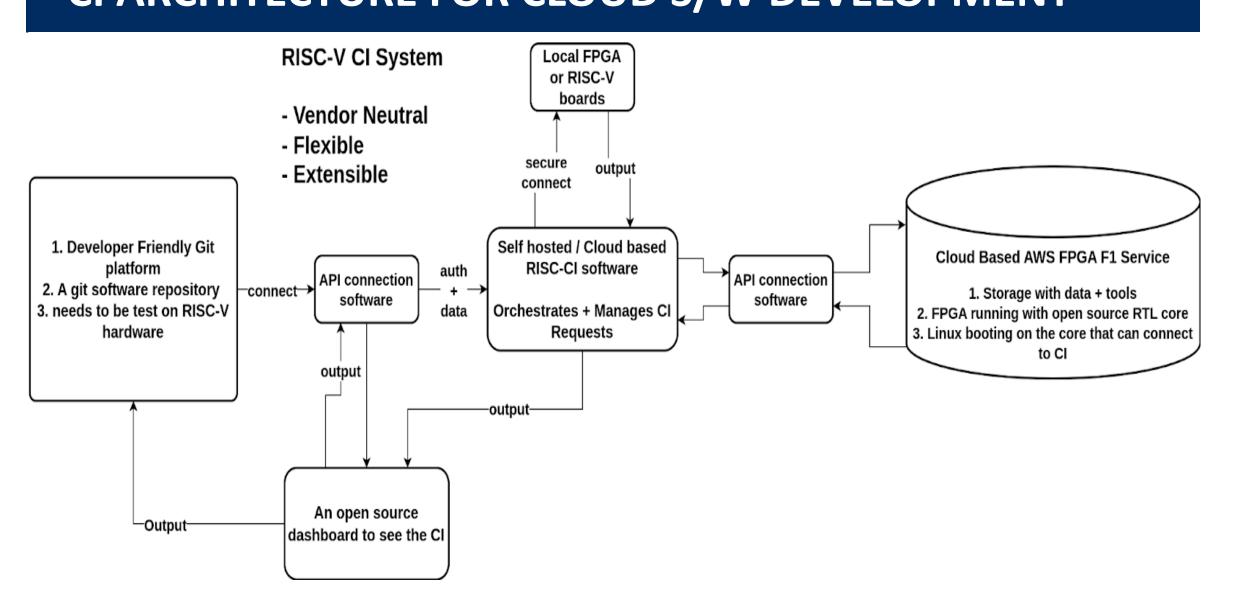
### HARDWARE CONFIGURATION

- 2-8 core CVA6 implementations on local and cloud-based (AWS F1) FPGA
- Appropriate NoC, RAM, storage and peripherals.
- Initial two-core CVA6-Platform is supported with RV64GC core support.
- Migrate toward eight-core configurations, and advanced ISA features such as RVV Vector
- •The processor core and accompanying cache, NoC, and chipset elements available in permissively licensed open—source, community driven RTL repos.
- •TRL5 verification

### **SOFTWARE SUPPORT**

- Provide a vendor-neutral RISC-V platform which can evolve quickly to support new ISA features
- Cycle level timing accuracy supports driver development, cache intensive applications, and real time software
- Firmware including working boot, and working linux (buildroot and/or distros) with documentation.
- RISC-V profile RVA20U64 initially supported.
- RVA22U64 supported in future.

## CI ARCHITECTURE FOR CLOUD S/W DEVELOPMENT



# GET INVOLVED: CVA6 @ OPENHW GROUP

- CVA6 and Supporting technologies
  - 64-bit application class and 32-bit embedded class
  - Superscalar
  - Vector
  - Hypervisor
  - Cache
  - NoC
- Mature Community ecosystem
  - Fully open-source, permissive license
  - TRL5 verification using CORE-V Verif
  - Fully documented
  - Part of a suite of full open-source cores



