A Rocket Core with Radar Signal Processing Accelerators as Memory-Mapped I/O Devices

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Overview

The increasing demands for specialized computational capabilities in radar signal processing necessitate advanced solutions. The proposed system leverages a RISC-V-based radar signal processor generator designed to meet these growing requirements. At its gist, the system integrates a Rocket core with dedicated radar hardware accelerators configured as memory-mapped I/O devices. The radar processing unit can handle streaming data input, coming either from a frontend directly or memory, and accelerate the most demanding radar signal processing operations like FFT and CFAR detection. By enabling parallel data processing across multiple radar receivers, the system achieves low latency and high throughput. Additionally, the architecture supports flexible software post-processing following thresholding, ensuring the utilization of various application-specific specialized extraction algorithms.

Main System Features

- Based around Chipyard Framework
- Leverages Rocket Chip SoC generator:
  - support for RV32 and RV64 ISA cores
  - Rocket can be swapped with BOOM Core
  - parameterizable number of Rocket Tiles
  - Rocket Tiles can be swapped for various different Tiles containing some other cores (Ariane/CVA6 Core, Ibex Core, etc.)
- DRAM for storing larger radar data cubes
- Raw radar data samples can be received:
  - over LVDS lines from a Radar Front-End
  - from Ethernet to the memory and then via DMA from the memory to the Accelerator
- Processed data samples can be:
  - streamed out through a Gigabit Ethernet
  - streamed out via DMA to main memory

Accelerator Key Features

Radar Accelerator MM bus and I/O Interface:

- support for TileLink, AXI4, AHB or APB
- AXI4-Stream Input/Output (I/O) interface

Common DSP Block Features:

- Arbitrary precision of fixed-point I/O data
- Different rounding methods for SNR increase
- Optional pipeline registers for better timing

FFT Features:

- Pipelined radix-2^2 SDF with a radix-3 stage
- Both forward and inverse complex FFT
- Compile-time decimation options: DIF/DIT
- Bit/digit reversed or natural output order
- Arbitrary fixed-point twiddle factor data
- Different scaling and data growth options
- Zero padding to nearest 2^n or $3 \cdot 2^{n-1}/2$

Supported CFAR algorithms:

- Sum, SO and GO CA-2D-CFAR
- OSCA 2D-CFAR
- CASO 2D-CFAR

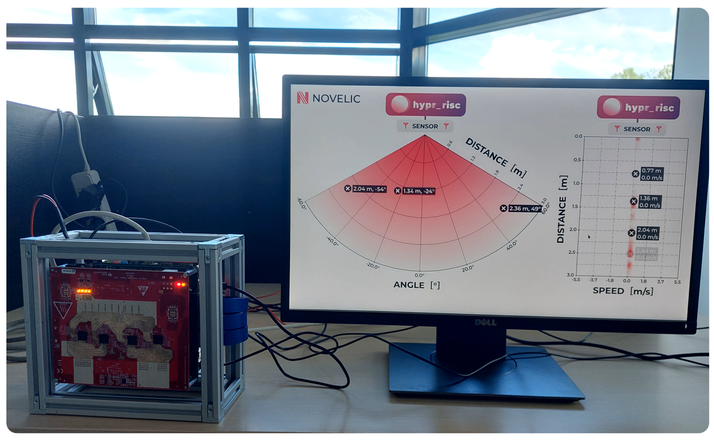
Supported Window Functions:

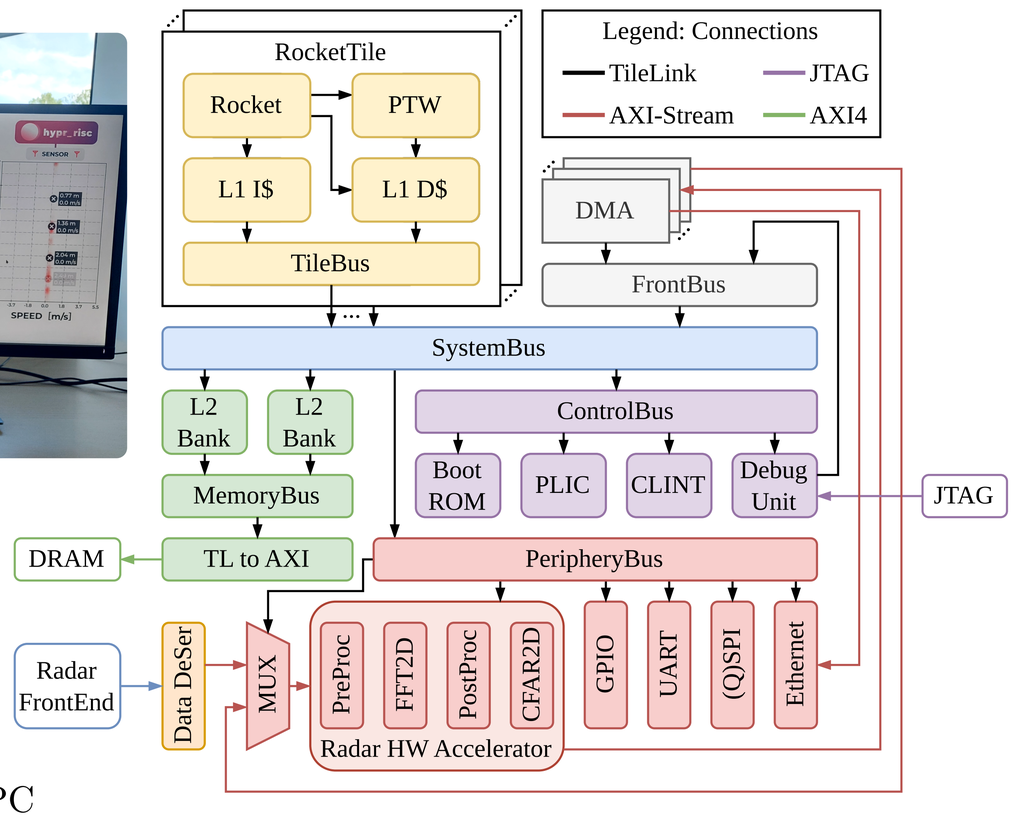
- Hann, Hamming, Blackman, Triangular,... as well as an arbitrary user specified window

Parameterizable number of:

- range and Doppler 2D-FFT DSP chains

Heterogeneous Radar Processor Block Diagram and Demonstrator

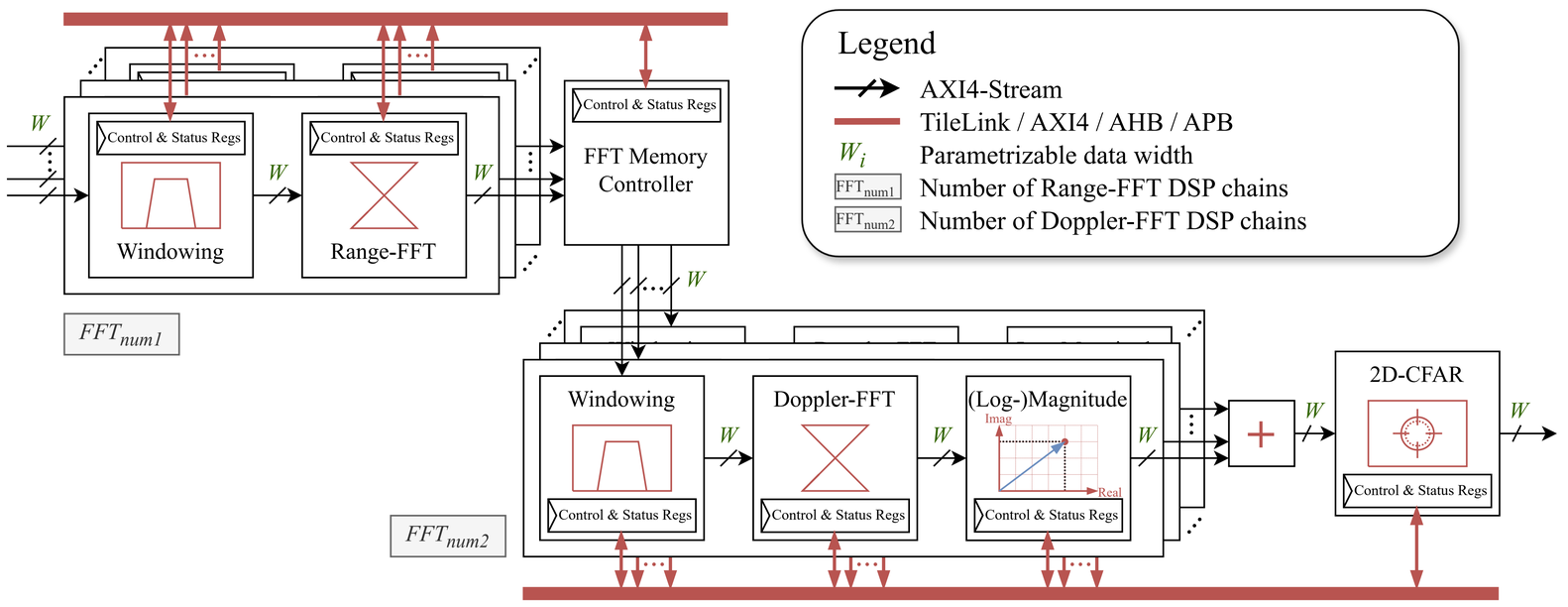




Developed hardware demonstrator:

- Radar Front End (TI AWR2243)
  - $[N = 1 \dots 12]$ TX channels
  - $[M = 1 \dots 16]$ RX channels
- Digilent Nexys Video FPGA
- Gigabit Ethernet connection to PC
- Up to 900 Mb/s of data per RX channel
- Range-Azimuth and Range-Doppler PC plotting

Radar Signal Processing Accelerator Block Diagram



Conclusions and Future Work

Developed Radar Processor is designed to be flexible, scalable, and adaptable to various Radar Front Ends, i.e., to be radar front end agnostic, with optional DRAM support for handling larger radar data matrices/cubes. The radar accelerator supports both transmitter time-division multiplexing (TDM) and beamforming modes, fixed-point arithmetic, and is run-time reconfigurable.

Current and future work includes:

- Direct frontend chirp configuration setup from the radar processor
- Migration from MMIO to a fully-fledged co-processor through RoCC interface
- Custom instruction set architecture (ISA) extension and ASIC chip implementation in nm CMOS

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