RISC-V Core and SoC Verification
Advanced Test Generation for RISC-V
Architectural and Micro-architectural Verification

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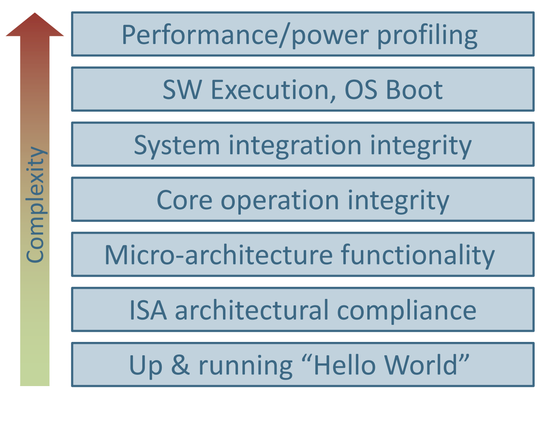
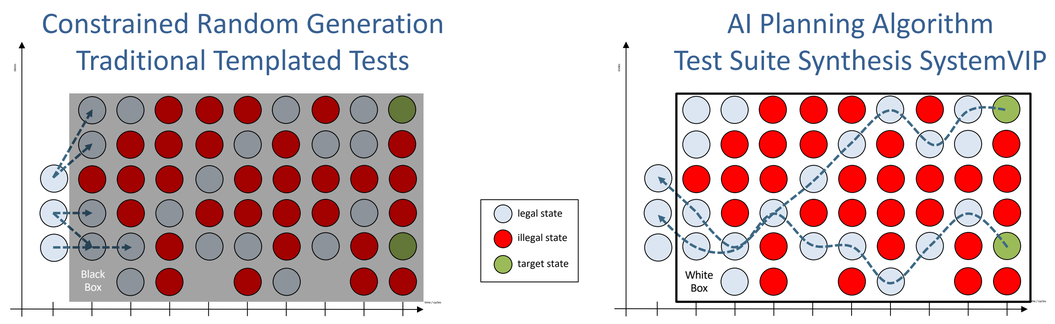
RISC-V Verification Challenges

- Ultrahigh quality expectation
  - ARM: 10^{15} verify cycles per core
- RISC-V special requirements
  - Custom instructions, ISA compliance, architecture range
- Different cores, different needs
  - Embedded vs App vs clusters, etc.

Common RISC-V verification "stack"



Synthesized vs Template RISC-V SystemVIP



AI planning algorithms, Compounded cross tests, Concurrent test scheduling

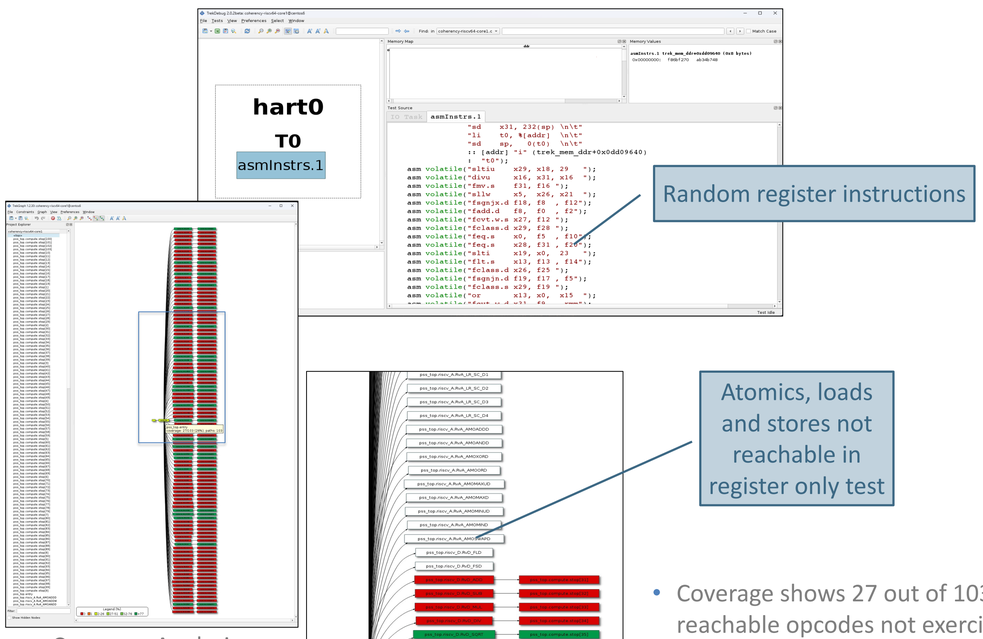
Synthesis amplifies coverage and bug hunting

RISC-V Core Assurance Verification

Core Test Content

Random Instructions	Do instructions yield correct results
Register/Register Hazards	Pipeline perturbations dues to register conflicts
Load/Store Integrity	Memory conflict patterns
Conditionals and Branches	Pipeline perturbations from synchronous PC change
Exceptions	Jumping to and returning from ISR
Asynchronous Interrupts	Pipeline perturbations from asynchronous PC change
Privilege Level Switching	Context switching
Core Security	Register and Memory protection by privilege level
Core Paging/MMU	Memory virtualization and TLB operation
Sleep/Wakeup	State retention across WFI
Voltage/Freq Scaling	Operation at different clock ratios
Core Coherency	Caches, evictions and snoops

Random Instruction Test and Coverage



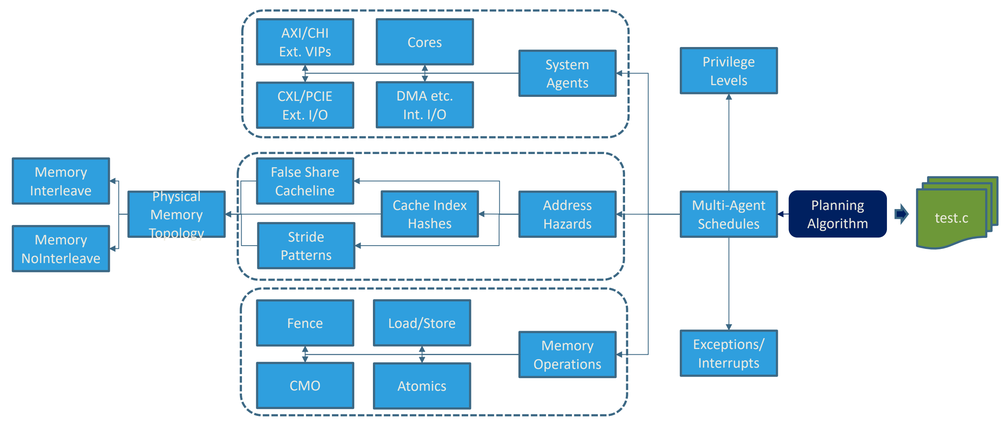
- Coverage shows 27 out of 103 reachable opcodes not exercised
- Atomics, loas & stores not reachable in randomized register test

RISC-V SoC Ready Verification

SoC Test Content

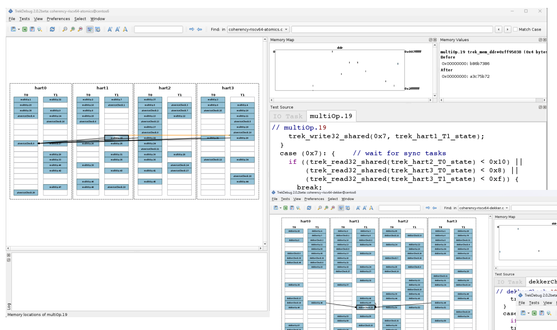
Random Memory Tests	Test Cores/Fabrics/Memory controllers across DDR, OCRAM, FLASH etc
Random Register Tests	Read/write test to all uncore registers
System Interrupts	Randomized interrupts through CLINT
Multi-core execution	Concurrent operations on fabric and memory
Memory ordering	For weakly order memory protocols
Atomic operation	Across all memory types
System Coherency	Cover all cache transitions, evictions, snoops
System Paging/IOMMU	System memory virtualization
System Security	Register and Memory protection across system
Power Management	System wide sleep/wakeup and voltage/freq scaling

SoC Cross Test Compounding Multiplication



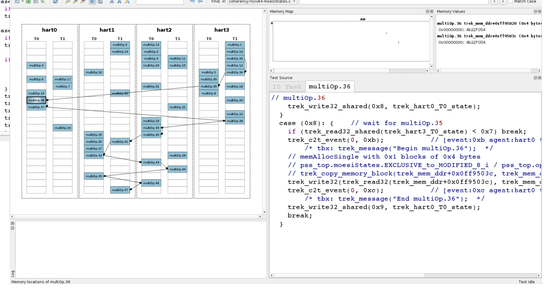
Test Examples That Reveal Hard-to-Predict Bugs

Atomics Tests



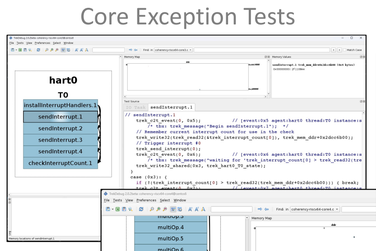
Memory Ordering Tests

Multicore Moesi States

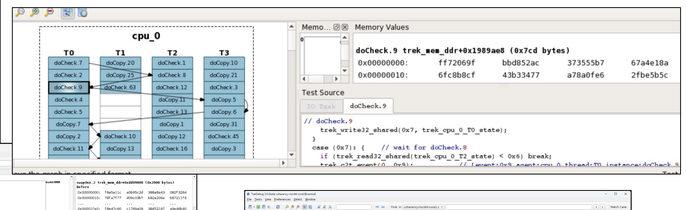


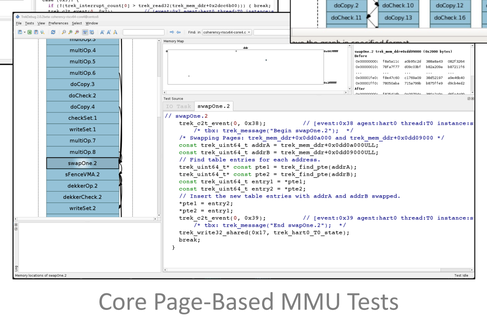
Advanced Core Level Testing Examples: Coverage Multiplication

Core Exception Tests

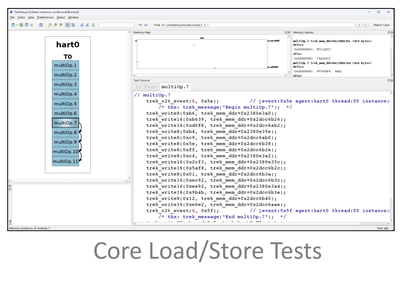


Core Integrity: 1 Core, 4 HART Resource Tests





Core Page-Based MMU Tests

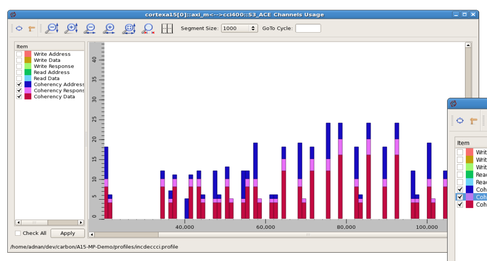


Core Load/Store Tests

Bugs and Coverage

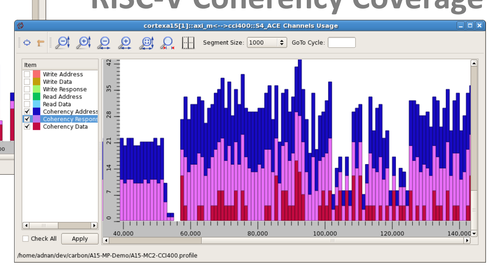
Examples of Recent Bug Discoveries

- Page fault mis-match in RISC-V SoC
- RISC-V fence instruction specification misunderstanding
- Coherent Mesh Network (CMN) programming issues
- Misconfigured ARM CMN pin to enable coherent traffic
- DDR model unable to handle AXI "wrap" transactions
- Common cache line access reveals deadlock
- Custom instruction bugs discovered by stress tests
- Results mismatch with ultrawide address strides
- Incorrect exception for guest virtual address[63:38] = 0x1ffffff
- Bad mcause value for guest physical address[63:31] != 0x0



Manual Test RISC-V Coherency Coverage

Synthesis SystemVIP RISC-V Coherency Coverage



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