

TitanSSL: Towards Accelerating OpenSSL in a Full RISC-V Architecture Using OpenTitan



¹Department of Electrical, Electronic, and Information Engineering (DEI) – University of Bologna, Italy ²Department of Control and Computer Engineering (DAUIN) – Polytechnic of Turin, Italy

alberto.musa@unibo.it



Motivation and Contribution

- The rapid evolution of cyber-physical systems (CPS) demands robust security measures. Utilizing OpenTitan in open-hardware
 System-on-Chip (SoC) technology offers a promising avenue for enhancing security, especially in accelerating cryptographic operations.
- Introduction of **TitanSSL**, <u>a software stack leveraging OpenTitan's</u> <u>hardware accelerators for cryptographic tasks</u>. This addresses the challenge of providing <u>a secure backend for OpenSSL within the SoC</u> <u>architecture</u>. Additionally, <u>comprehensive evaluation of TitanSSL's</u> <u>performance</u> reveals insights into the trade-offs between computational

Table 1: TitanSSL results in terms of cycles per byte.

Test	Cycles per Byte			Speedup	Overhead
	OpenSSL	TitanSSL	SCF	opecuup	overnead
		sh	a		
16 B	462	877	61	0.5	93.1 %
64 B	216	231	27	0.9	88.2 %
$256\mathrm{B}$	127	71	20	1.8	72.1%
$1024\mathrm{B}$	104	31	18	3.4	41.6 %
		ae	s		
16 B	155	947	136	0.2	85.6 %
64 B	145	270	67	0.5	75.2%
$256\mathrm{B}$	142	101	51	1.4	50.1 %
$1024\mathrm{B}$	141	60	47	2.4	21.2%
		rsa-pu	ıblic		
512b	2 4 3 0	2678	2 3 9 6	0.9	10.5%
$1024 \mathrm{b}$	3815	2 2 50	2109	1.7	6.3 %
2048 ь	5126	2790	2720	1.8	2.5%
		rsa-pr	ivate		
$512 \mathrm{b}$	30 518	8618	8 337	3.5	3.3 %
$1024 \mathrm{b}$	68 531	23016	22875	3.0	0.6%
2048b	193 955	78140	78 070	2.5	0.1 %

overhead and speed-up.

Security Implications & Assumptions

- Integration of OpenTitan as a Root-of-Trust enhances the overall security posture of the SoC, ensuring secure boot and isolation of critical operations. Leveraging hardware accelerators for cryptographic tasks improves resistance against side-channel attacks and enhances system resilience. TitanSSL orchestrates secure communication between the application processor and the security controller, mitigating potential vulnerabilities in cryptographic operations.
- Assumptions include <u>the integrity and reliability of OpenTitan's hardware</u> <u>components</u>, proper implementation and configuration of TitanSSL components for <u>secure communication and key management</u>, <u>and trust in</u> <u>the underlying firmware and software stack</u>, **including OpenSSL**, for handling cryptographic requests securely.

Summary of Findings

- Significant speed-ups observed in cryptographic operations, with SHA-256 and AES-256-CBC exhibiting enhancements of 3.4x and 2.4x, respectively. RSA operations also demonstrated improvements, achieving speed-ups of approximately 1.8x and 3.5x.
- Despite overhead, TitanSSL efficiently utilizes OpenTitan's hardware accelerators, showcasing its effectiveness in accelerating cryptographic workloads while securely operating within OpenTitan's environment and leveraging its root-of-trust capabilities

[1] Bryan Parno et al. "Roots of Trust". In: Bootstrapping Trust in Modern Computers. New York, NY: Springer New York, 2011, pp. 35–40.
[2] Maicol Ciani et al. "Cyber Security aboard Micro Aerial Vehicles: An OpenTitan-based Visual Communication Use Case". In: 2023 IEEE ISCAS. 2023.
[3] F. Zaruba et al. "The Cost of Application-Class Processing: Energy and Performance Analysis of a Linux-Ready 1.7-GHz 64-Bit RISC-V Core in 22-nm FDSOI Technology". In: IEEE VLSI (2019)
[4] IowRISC CIC. OpenTitan Official Documentation. https://opentitan.org/book/doc/introduction.html. 2019.

[5] Pasquale Davide Schiavone et al. "Slow and steady wins the race? A comparison of ultra-low-power RISC-V cores for Internet-of-Things applications". In: PATMOS. 2017.

[6] Scott Johnson et al. "Titan: enabling a transparent silicon root of trust for cloud". In: Hot Chips: A Symposium on High Performance Chips. Vol. 194. 2018. 2 RISC-V Summit Europe, Munich.

