# Improvement of the Execution Cycles Estimation of Application SW in Cross-Compiled Simulation of RISC-V Platforms Using AI

Raul Gomez, Hector Posadas, David Aledo & Eugenio Villar

TEISA Dpt., University of Cantabria, Santander, Spain

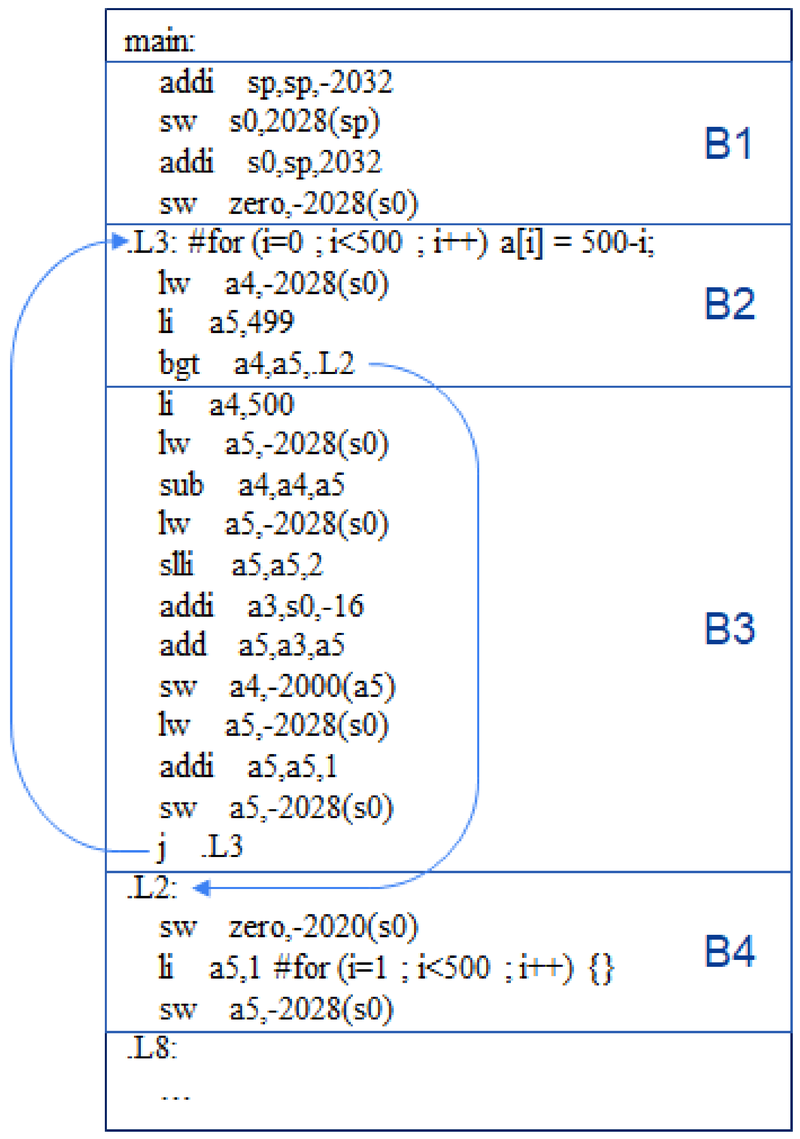
## Problem statement

The number of clock cycles required by a processor to execute a certain code is the addition of the number of cycles required to execute the instructions and the clock cycles provoked by cache misses.


How many clock cycles will be required to execute each basic block?

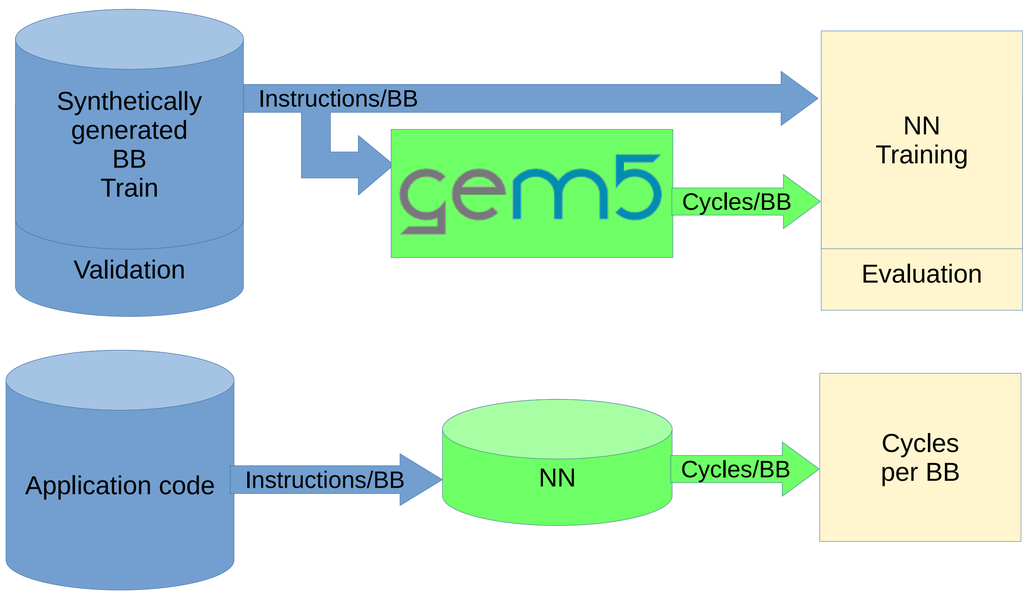
## Related work

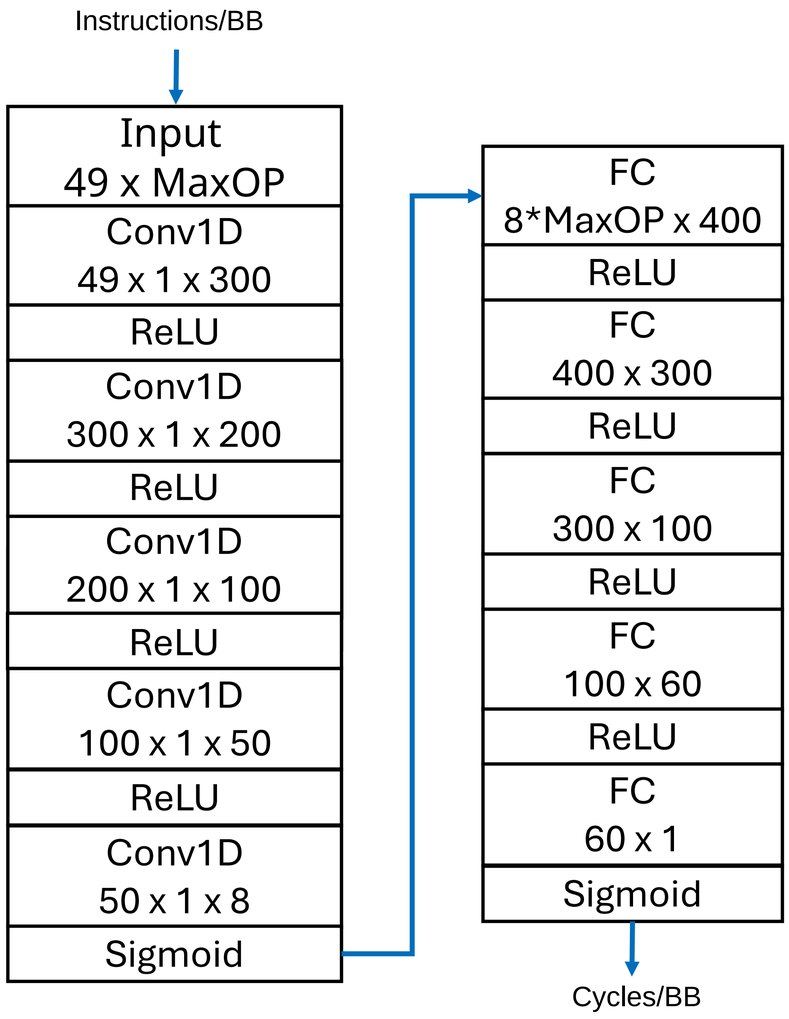
| | |
|---|---|
| No timing estimation | Untimed simulation with a 100% error. |
| One clock cycle per instruction | Approximate simulation using the average number of cycles it would take to execute any given instruction. |
| Constant cycles per instruction | Similar to the previous, but more precise by differentiating between instructions and the number of cycles for each. |
| Algorithmic calculation | Similar to the previous, but more precise by taking into account dependencies among instructions and even out-of-order execution, it requires knowledge of the actual CPU architecture and has the development for each architecture. |

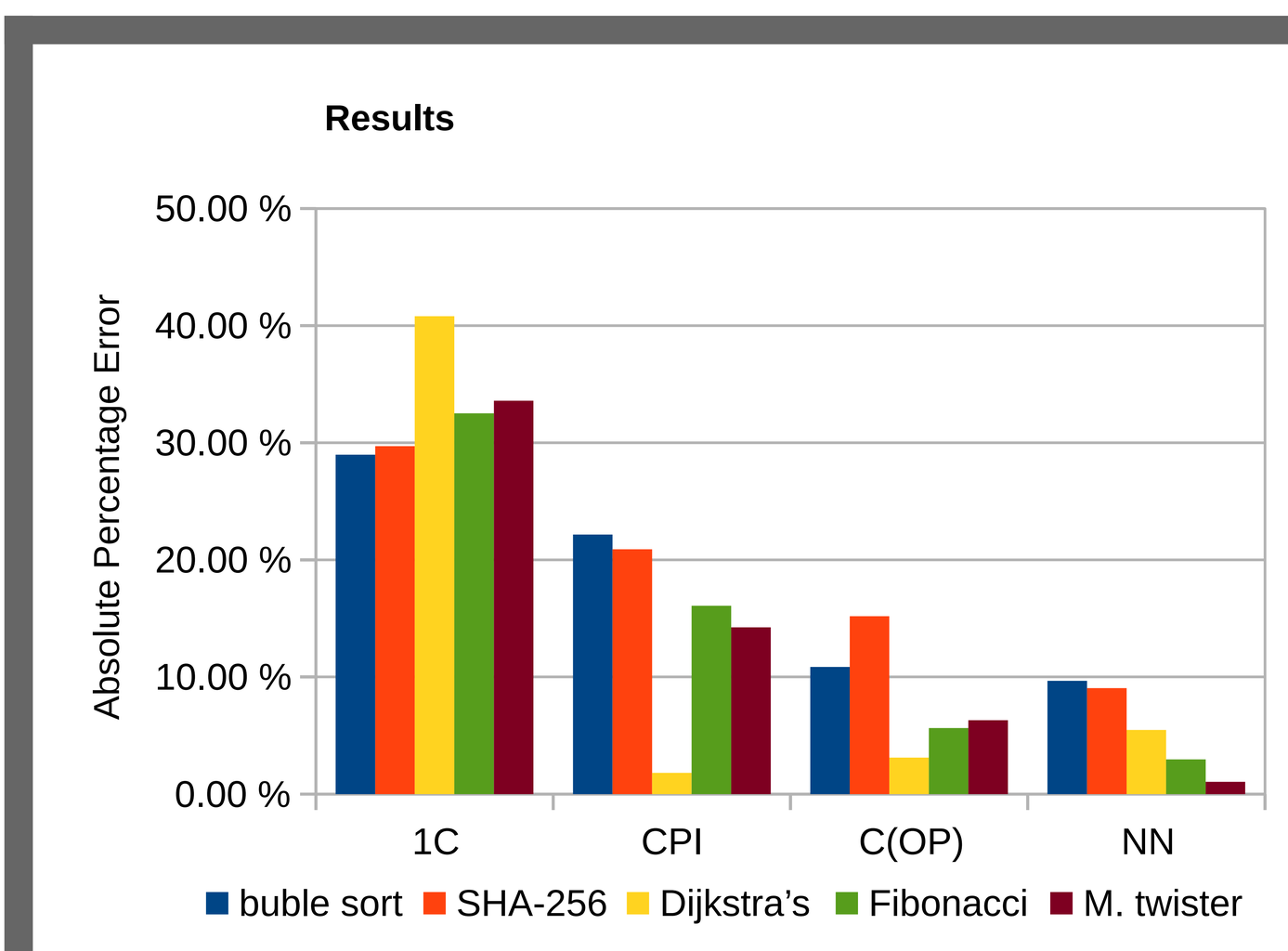



## AI-Based Methodology:

A neural network is trained to predict the number of cycles required by a BB (basic block) based on the instructions it contains. The neural network takes information about the instructions in the BB as input and produces a more precise estimation of the execution time. This not only allows for the consideration of dependencies between instructions but also enables the evaluation of the performance impact with a high degree of accuracy that would result from out-of-order execution, pipeline behavior, etc.




AIDOaRt
ECSEL Joint Undertaking
GOBIERNO DE ESPAÑA
MINISTERIO DE CIENCIA E INNOVACIÓN
Comisión Europea