Three RISC-V SoCs in Three Years

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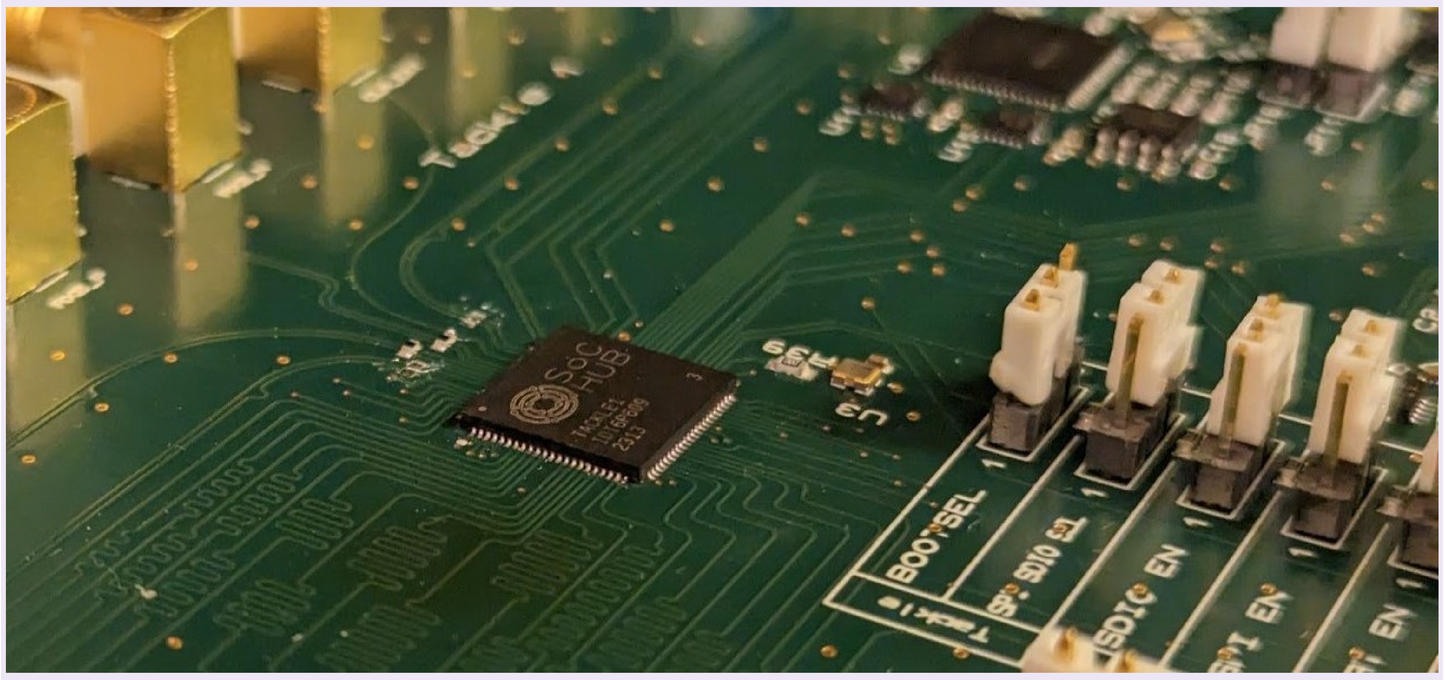
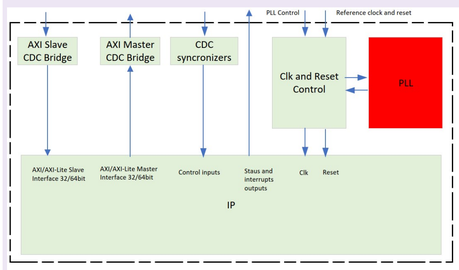
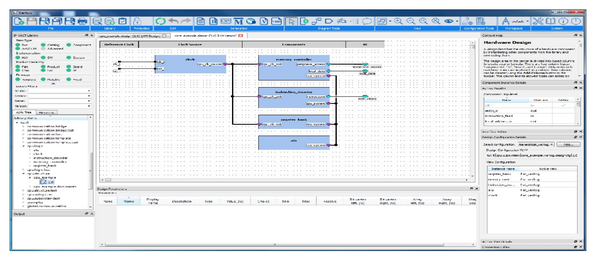


- A joint effort between Tampere University and experienced local companies
- Rapid development cycle
- One chip per year cadence
- Industry-level quality
- Three SoCs taped out between 2020 - 2023: Ballast (15mm^2), Tackle (4mm^2) and Headsail (25mm^2), on 22nm CMOS technology.

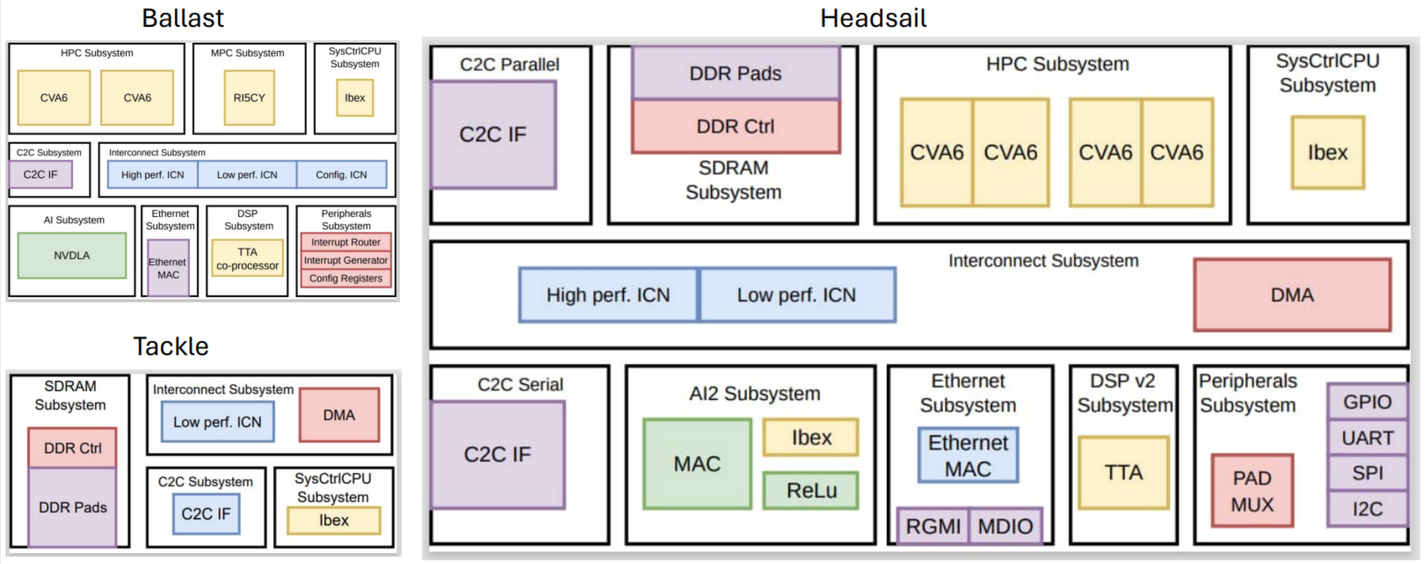
Methodologies





- **Template-based sub-system architecture**
  - On-chip interconnect interfaces, Clock Domain Crossings and clock tree harmonization
- **Physical Design**
  - The selected sub-system architecture enabled a hierarchical physical design flow and accelerated project execution. The physical design activities for sub-systems were run concurrently.
- **IP-XACT modeling of the SoC with Kactus2 tool**
  - SoC IP-XACT models enabled the generation of RTL and SW for subsystem interfaces.
- **Verification**
  - HW/SW co-simulation (C & RUST), UVM testbenches and FPGA prototyping.

RISC-V SoCs



- Reuse of high-quality open-source RISC-V CPU cores and applying efficient methodologies accelerated the development time.
- The importance of having high-quality documentation available when using existing open-source IPs efficiently was emphasized.

	Ballast		Tackle		Headsail	
Sub-system	**Freq.**	**Area (inc. mem.)**	**Freq.**	**Area (inc. mem.)**	**Freq.**	**Area (inc. mem.)**
64b RISC-5 CVA6	500MHz	5,3mm^2 (2x cores)	NA	NA	1GHz	7mm^2 (4x cores)
32b RISC-V CV32E40P	500MHz	2,5mm^2	NA	NA	NA	NA
32b RISC-V IBEX	30MHz	0,35mm^2	30MHz	0,32mm^2	30MHz	0,42mm^2
32b RISC-V DSP	600MHz	0,95mm^2	NA	NA	1GHz	0,74mm^2
C2C Parallel	400MHz, Ios 100MHz	1mm^2	NA	NA	400MHz, Ios 100MHz	1mm^2
C2C Serial	NA	NA	2,85GHz	0,3mm^2 (excl. analog macros)	3GHz	0,4mm^2 (excl. analog macros)
AI: NVDLA	750MHz	2,6mm^2	NA	NA	NA	NA
AI: DLA	NA	NA	NA	NA	900Mhz	9,4mm2
1G ETH	125MHz	0,7mm^2	NA	NA	NA	NA
2x1G ETH	NA	NA	NA	NA	125MHz	1,5mm^2
LP-DDR2 SDRAM	NA	NA	533MHz	1,5mm^2 (excl. analog macros)	533MHz	1,5mm^2 (excl. analog macros)
ICN+ DMA+ Shared SRAM	1200/637/166MHz	2,37mm^2 (No DMA nor SRAM)	533MHz	0,9mm^2	1Ghz	3,8mm^2

Note #1:	reuse of the open-source Pulp-Platform
Note #2:	SoC-Hub developed IP
Note #3:	NVIDIA open-source IP

Effort analysis

- **The RISC-V ecosystem is keen on prototyping and productizing RISC-V-based SoCs, but a published analysis of the required effort to do so did not exist.**
- As a result we reported the resources needed for developing chips, leveraging open-source RISC-V CPUs and many new SoC platform IPs.

	Ballast	Tackle	Headsail
Person months	133	73	137
Personel	22	18	21
Calendar time (months)	12	12	8

Note #1:	Person months are normalized to equivalent expert months.
Note #2:	Some of the team members worked part-time.
Note #3:	Calendar time is recorded from architectural definition to tapeout of the chip

- An effort analysis was conducted which focused on the hardware team.
- The analysis included the work done within design, verification, physical design, FPGA prototyping, project management and IT infrastructure maintenance.
- Project execution time includes the time from architectural definition to tapeout.

Conclusion

- Our success in taping out three SoCs within a three year period demonstrates that a fast SoC development cycle can be achieved by reusing open-source RISC-V cores.

Tampere University

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sochub.fi
Kactus2 IP-Xact tool
Custom RISC-V compatible DSP
Ballast SoC