Spike as a Reference Model in CORE-V-VERIF

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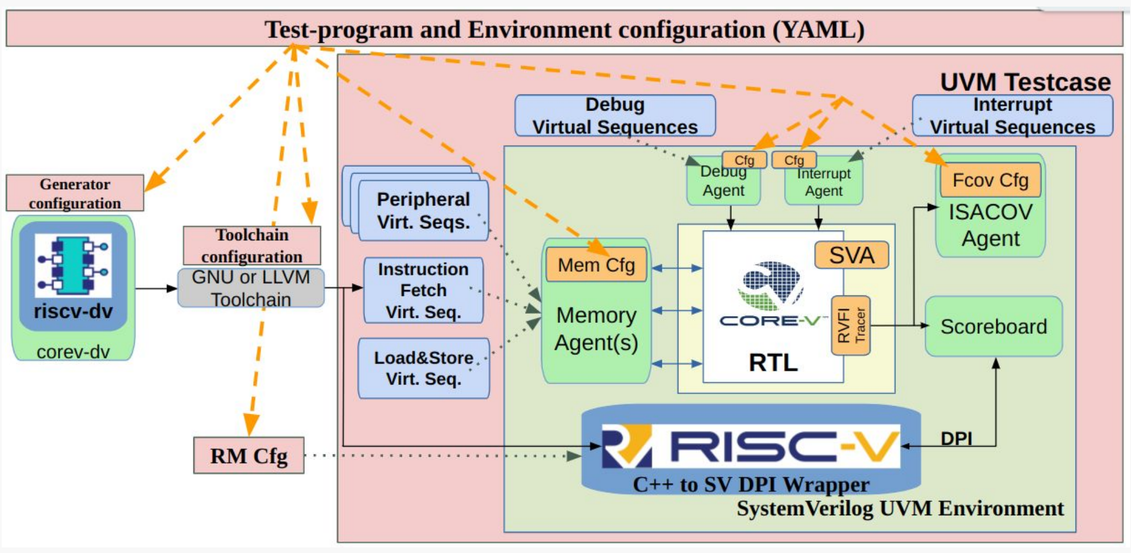
What's CORE-V-VERIF?

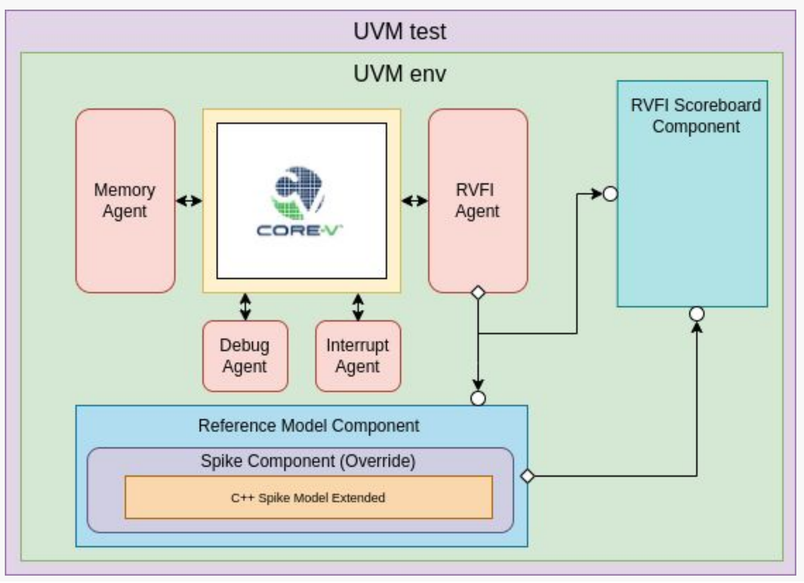
Beginning in 2020, OpenHW Group has been developing CORE-V-VERIF to support both proprietary and open-source Reference Models, aiming for comprehensive functional verification of RISC-V cores. The use of Spike (riscv-isa-sim) is a milestone towards fully open-source industrial-grade verification, a key goal for many stakeholders and European Projects such as TRISTAN.



Spike as a Reference Model

The key considerations involved in using Spike as an RM:

- Exposing the architectural state (PC, GPRs and CSRs) of both the RTL and RM to the Scoreboard.
- Handling asynchronous traps such as interrupts and debug requests.
- Configuring Spike to match implementation decisions of the specific Core-Under-Verification.



Exposing Architectural State

Core-Under-Verification: The OpenHW Group has defined a extension of the YosysHQ RISC-V Formal Interface (RVFI). This extension exposes the architectural state of the core.

Spike API: The C++ interface to Spike's internal state is not considered a public API. In CORE-V-VERIF we handle this by defining a set of functions to modify and expose Spike state.

Asynchronous Traps

Interrupts: When the core receives an interrupt and jumps to the handler, the reference model is notified to keep track of the core's actions. In the reference model, when the RVFI trap field is set high, the MIP register is constructed by examining the core's MCAUSE.

Debug: When the RVFI dbg field is set and it is a external debug request it will be injected in the reference model and both will enter in debug mode.

Configuring Spike

- The RISC-V ISA allows for multiple implementation decisions.
- The RTL and RM must make the same implementation decisions or their architectural state may diverge.
- The verification environment manages the Spike configuration by implementing a set of parameters that adjust the simulation of the reference model before its instantiation. This allows for modifications in the simulation, such as the behavior of CSRs or SoC parameters.

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