Accelerating RISC-V Verification

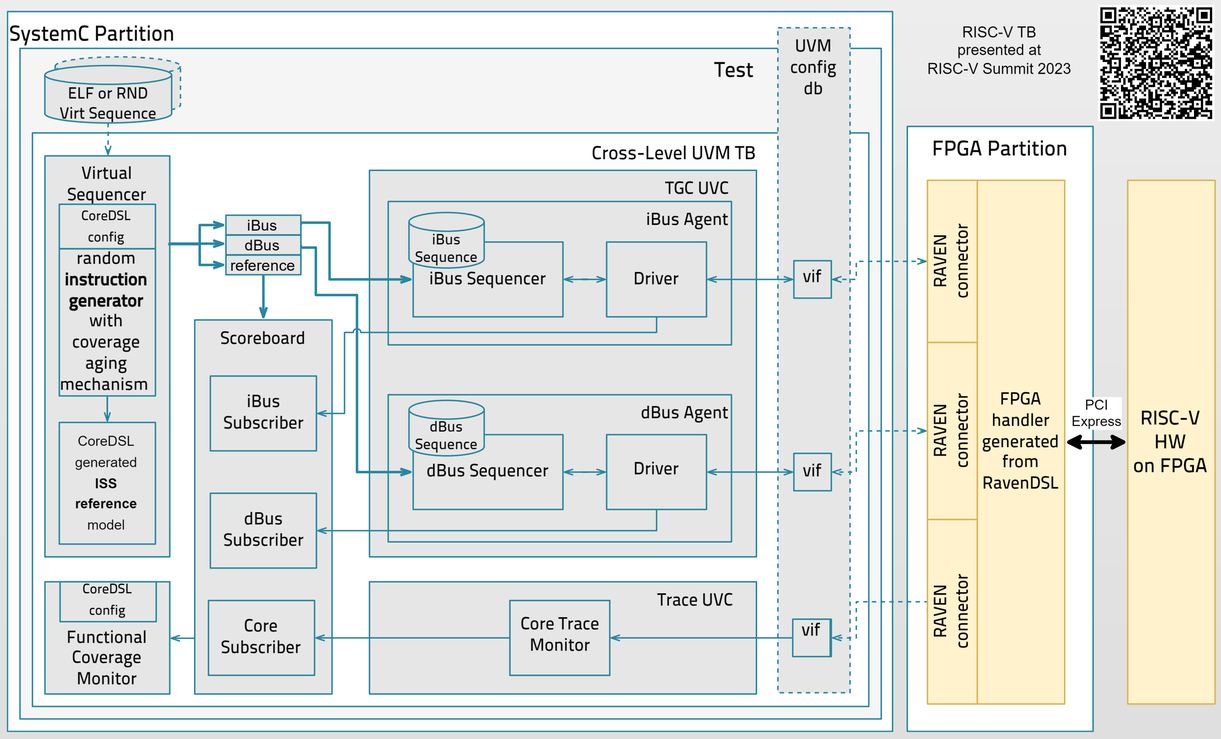
Speedup core verification through scalable hybrid FPGA Co-Simulation in 4 simple steps

1 **RISC-V core description in RavenDSL**

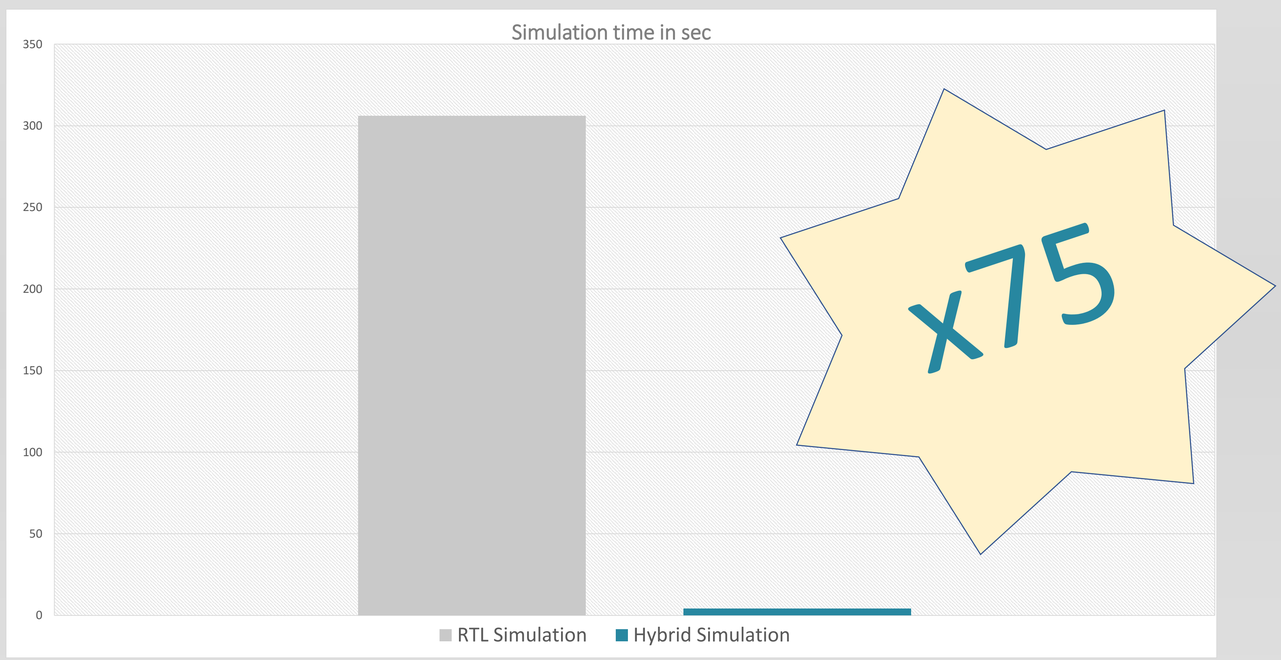
```
1   import axi4full;
2   import signal;
3   import reset;
4
5   dut TGC5M_AXI4ID;
6       clocks
7           Clock#(100) clk;
8       endclocks
9       resets
10          ResetAgent#(10)(ACTIVE_HIGH) reset;
11      endresets
12      SignalInAgent#(1)  timIrq;
13      SignalInAgent#(1)  swIrq;
14      SignalInAgent#(1)  extIrq;
15      SignalInAgent#(1)  extIrqSv;
16      SignalInAgent#(64) rdtime;
17      AXI4MasterAgent#(32,64,1,0) iBus;
18      AXI4MasterAgent#(32,64,3,0) dBus;
19  enddut
```

2 **Automatic generation of the FPGA partition**

3 **Connection of the FPGA Partition**



4 **Automatic generation of the bitstream**



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