Automated Synthesis of a Multicore RISC-V SoC with Interconnect Customized for Dataflow Requirements Based on LiteX

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Introduction & objectives

- **Dataflow modeling**: Facilitates software-to-hardware translations, exploiting architecture resources for application requirements [3].
- **Design Space Exploration (DSE)**: Automates system design decisions and remaps applications to fixed resources.
- **LiteX Framework**: LiteX [2] offers customized SoC generation, supporting peripherals and CPU cores like RISC-V for rapid prototyping

The objectives are:

- **Automate SoC Design:** Use LiteX for creating custom SoCs tailored to dataflow applications
- **Bridge Simulation and Execution:** Reduce mismatches between simulation and real system execution

Scratchy structure

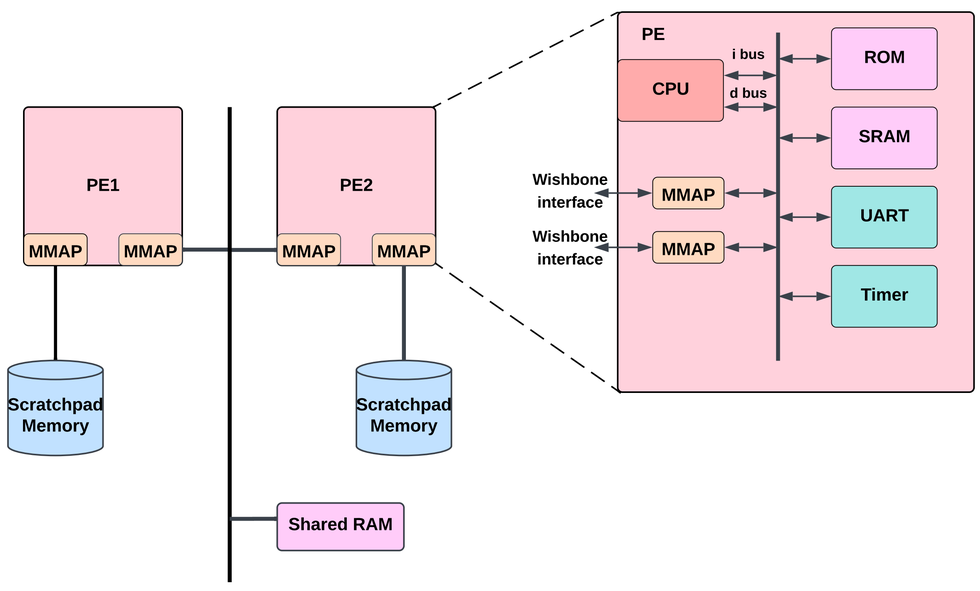


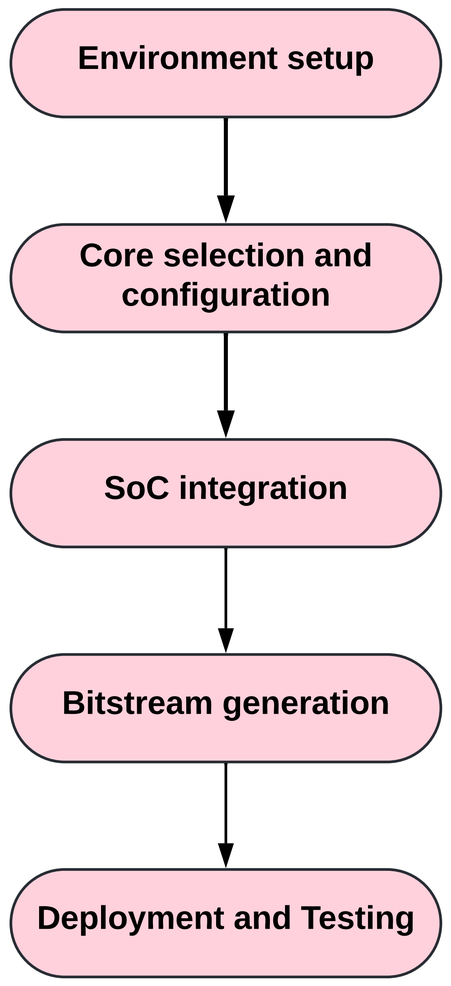
Figure 1. A LiteX scratchpad-based dual-core architecture.

1. **Scratchy aims at tailoring computing resources of a multiprocessor to the needs of a Synchronous Dataflow (SDF) modeled application.**
2. **Scartchy is lightweight, with little overhead for inter-processors communication.**
3. **A 2-core scratchy fits a DE10-lite MAX10 Intel FPGA, consuming less than 30 % of logical elements.**

Results

- **Efficient SoC Creation:** The dual-core architecture is functional on DE10-LITE Intel FPGA [1], and Xilinx ZCU102 platforms.
- **Customizable Resources:** The SoC supports dataflow applications by providing customizable resources to match data streams.
- **Impact of LiteX:** Demonstrated potential for automating and optimizing SoC design for dataflow applications.

Methodology



- **Environment setup:** install LiteX, drivers, Vivado, ...
- **Core selection and configuration:** selection of the RISC-V cores and configure the size of ROM, SRAM, ...

Figure 2. LiteX SoC creation Steps

Challenges

- Expand the number of cores.
- Integrate external memory and enable near-memory computing for stream applications.
- Extend the architecture creation process in PREESM to utilize LiteX for automatically generating SoCs optimized for dataflow applications.

References

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