XiangShan: Empowering Open-Source RISC-V Innovation with High Performance Processor and Agile Infrastructure

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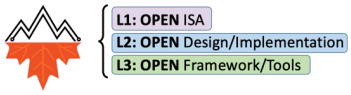
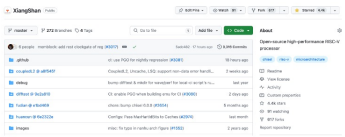
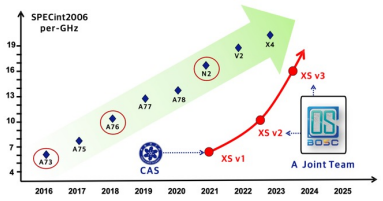
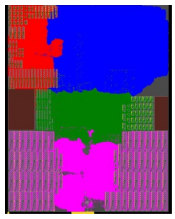
XiangShan Overview

XiangShan is an **open-source high-performance RISC-V processor** project introduced in 2020, aiming to establish a leading platform with end-to-end **agile development flows and tools** for commercial and research applications.





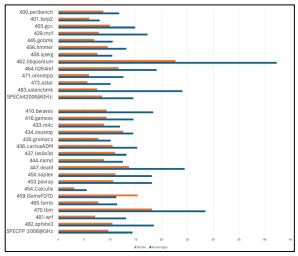




Building upon the success of the first generation Yanqihu and the second generation Nanhu, the third generation Kunminghu has completed its RTL design and is ready for tape-out. The latest version of XiangShan achieves a normalized score of **45 at 3GHz on SPECint 2006**. With the performance comparable to ARM Neoverse N2, it is **the highest performing open-source processor** to our knowledge.

Highlights in XiangShan V3

- **Functional Enhancement**
  - RV Vector/Hypervisor extension
  - CHI Interconnection
- **Performance Exploration**
  - 1.5x IPC of XS V2, 3GHz
  - Calibrated performance model
- **Functional Verification**
  - Hierarchical verification flow
  - Industrial-grade verification process



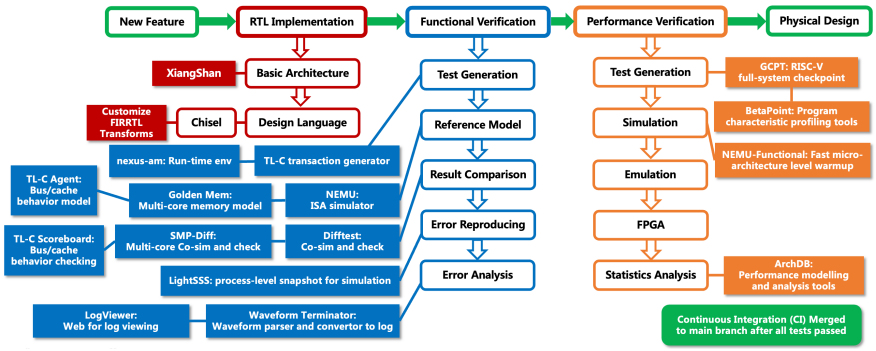
SPEC CPU2006/GHz performance of NH and KMH

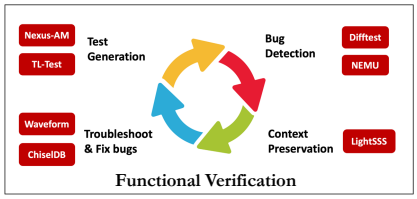
Real Chips

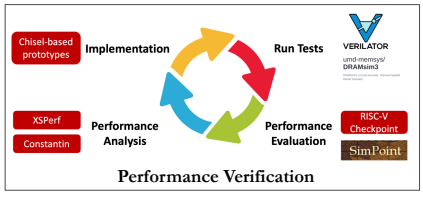
XiangShan V1(Y100)

XiangShan V2(N300)

Agile Development Toolchain

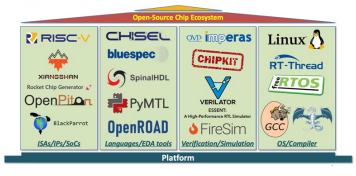






Outlook

- XiangShan **fills the gap in high performance** open-source processors
- With **three generations of optimization**, XiangShan meets the needs from both academia and industry
- **Agile verification tools** are involved early in the workflow, reducing the number of iterations and enhancing performance analysis to provide more opportunities for innovation



Together for a Shared Future!
To Lower the Barrier of Chip Development

Welcome to Join Us !

XiangShan Source Code Repo: https://github.com/OpenXiangShan
Docs: https://xiangshan-doc.readthedocs.io
Email: xiangshan-all@ict.ac.cn
Institute Website: https://www.bosc.ac.cn

Github Repository

WeChat Official Account