Application Specific ISA Extensions in RFID Edge Processing

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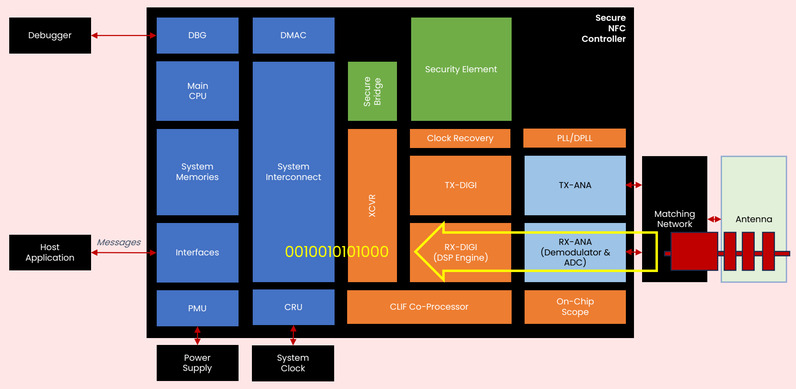
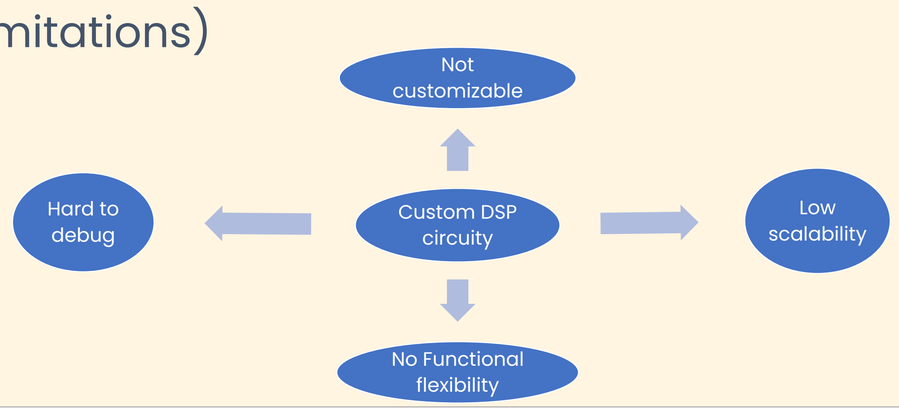
State of Art in NFC Modems Architectures

- Full custom digital logic solutions
- Massive use of DSP structures, configuration registry and debug infrastructure
- High functional density per silicon area
- Highly performing
- Hard-coded functionality
  - Reader and Card-Emulation modes
  - WLC
  - Runtime automatic gain, phase and DCO control loops



Problem Statement (State of Art limitations)

Any functional improvement or problem fix not solved by FW requires a silicon respin!

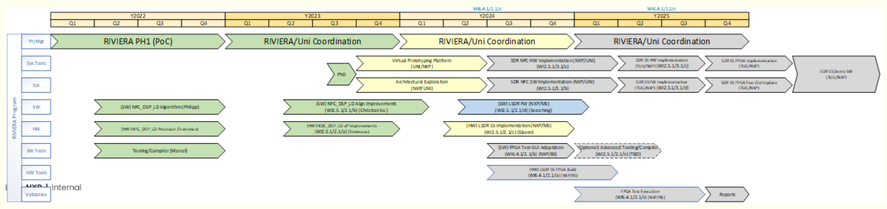


A novel architectural approach is necessary, that aims at:

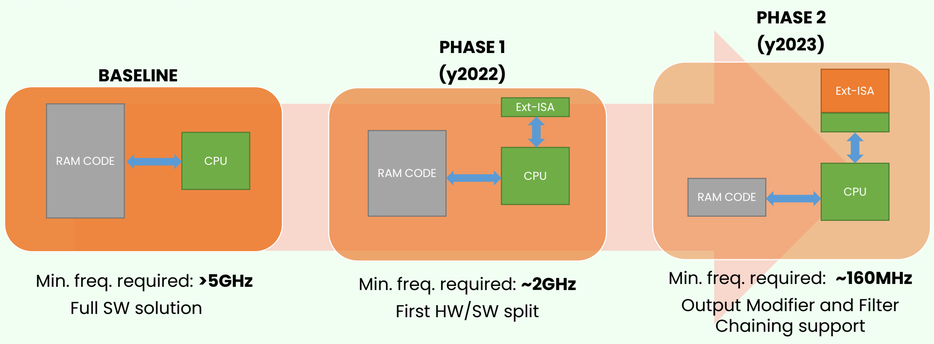
- Scalability
- In-field reconfiguration
- Testability

Students' Collaboration Plan (NXP RIVIERA)

- **RIVIERA** is the acronym for "**RI**SC-**V** **I**SA **E**xtensions for **R**FID **A**pplications".
- NXP Austria academical program run with **TU-Graz** and **Politecnico di Torino**.
- Supported by NXP France on FPGA proto board.
- Concept: Architectural investigations aiming to SW Defined Radio for NFC Applications.
- Duration: 4 years, mostly framed into TRISTAN Project.
- Multiple master, bachelor HW, SW and Validation thesis works.
- Status: 2 generations of master HW and SW student run.
- Next stage: MCU system build, mapping on FPGA, bring-up and validation.



Architectural Explorations



RISC-V co-processor instructions (Ext-ISA)

Description	Funct7 31 25	Rs2 24 20	Rs1 19 15	Funct3 14 12	Rd 11 7	Opcode 6 0	
clear_data	0	X	bank_index	0	X	0x2b	
clear_coeff	1	X	bank_index	0	X	0x2b	
set_nfeed	2	n_feed	bank_index	0	X	0x2b	
set_rounding	3	nbits_cut	bank_index	0	X	0x2b	
set_simd*	4	simd	bank_index	0	X	0x2b	Updated in Phase 2
load_data_mem	0	mem_addr	bank_index	1	X	0x2b	
load_coeff_mem	0	mem_addr	bank_index	2	X	0x2b	
load_data_reg	0	input_data	bank_index	3	X	0x2b	
load_coeff_reg	0	input_coeff	bank_index	4	X	0x2b	
exec_mac	0	X	bank_index	5	output	0x2b	
load_exec_data_mem	0	mem_addr	bank_index	6	output	0x2b	
load_exec_data_reg*	0	input_data	bank_index	7	output	0x2b	Updated in Phase 2

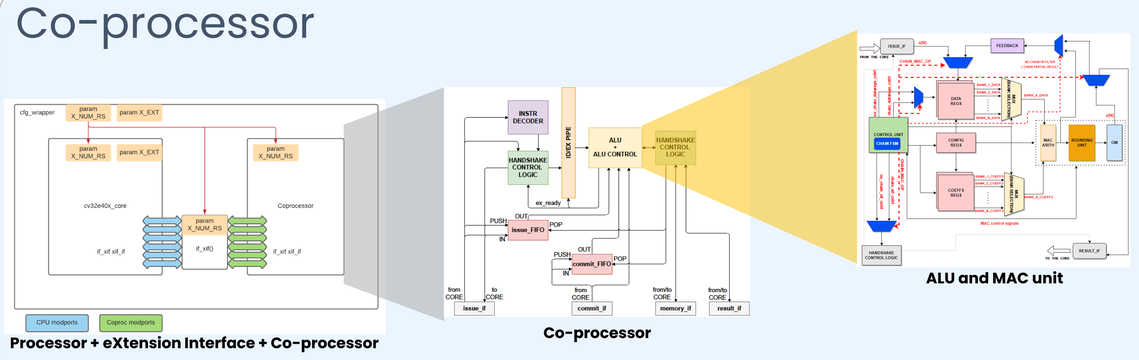
Open-Source Building Blocks

CV32E40X

An Open-Source Core fit for our needs

- RV32I: RV32I Base Integer Instruction Set
- RV32E: RV32E Base Integer Instruction Set
- Standard instruction set extensions:
  - C ⇒ Standard Extension for Compressed Instructions;
  - M ⇒Standard Extension for Integer Multiplication and Division;
  - Zicntr ⇒Standard Extension for Base Counters and Timers;
  - Zihpm ⇒ Standard Extension for Hardware Performance Counters;
  - Zicsr ⇒ Control and Status Register Instructions;
  - Zifencei ⇒Instruction-Fetch Fence.
- **eXtension Interface support (Xif)**
  - Main reason to choose this core version.

Co-processor

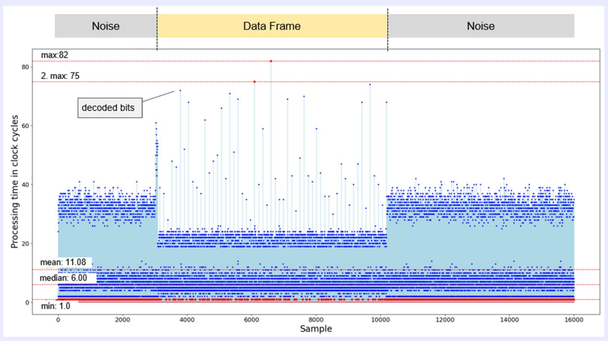


Processor + eXtension Interface + Co-processor

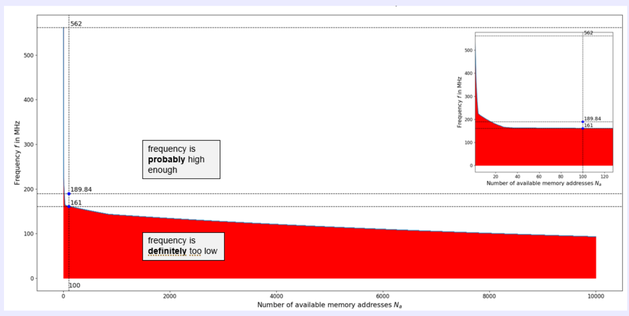
Co-processor

Proof of Concept

Sample versus clock cycles plot: maximum peak 82 clock cycles in the frame:



Results (PPA)



Relation between available buffer size vs minimum clock frequency (Na = 1 → fmin = 562 MHz, Na = 100 → fmin = 161 MHz).

Instance Name	Gate Count	Leakeage [mW]	Dynamic [mW]	Total [mW]
core_coproc_top	145846	0.90837	108.0708	108.97917
i_coproc	112246	0.737553	81.0562	81.793753
i_cv32e40x_core	33601	0.170816	26.934	27.104816

Gate count and Power results

per algorithm run	y2022	y2023	difference	speedup
number of instructions	705946	37253	-668693	18.95
number of clock cycles	2578982	177373	-2401609	14.54
frequency at Na=1	3212 MHz	562 MHz	-2650 MHz	5.72
frequency at Na=100	2189 MHz	161 MHz	-2028 MHz	13.60

Performance comparison

Next Steps

RIVIERA Phase-3 plan of record:

- Build of a MPU subsystem, based on the core + coprocessor;
- Development of a full SW stack to support the decoding algorithm;
- HW & SW integration on a virtual verification env (SV-UVM TB)
- Test env setup based on a FPGA prototyping platform;
- Validation and performance analysis.

TRISTAN WEBSITE

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