Enhanced LPDDR4X PHY in 12nm FinFET

RISC-V managed LPDDR4X PHY

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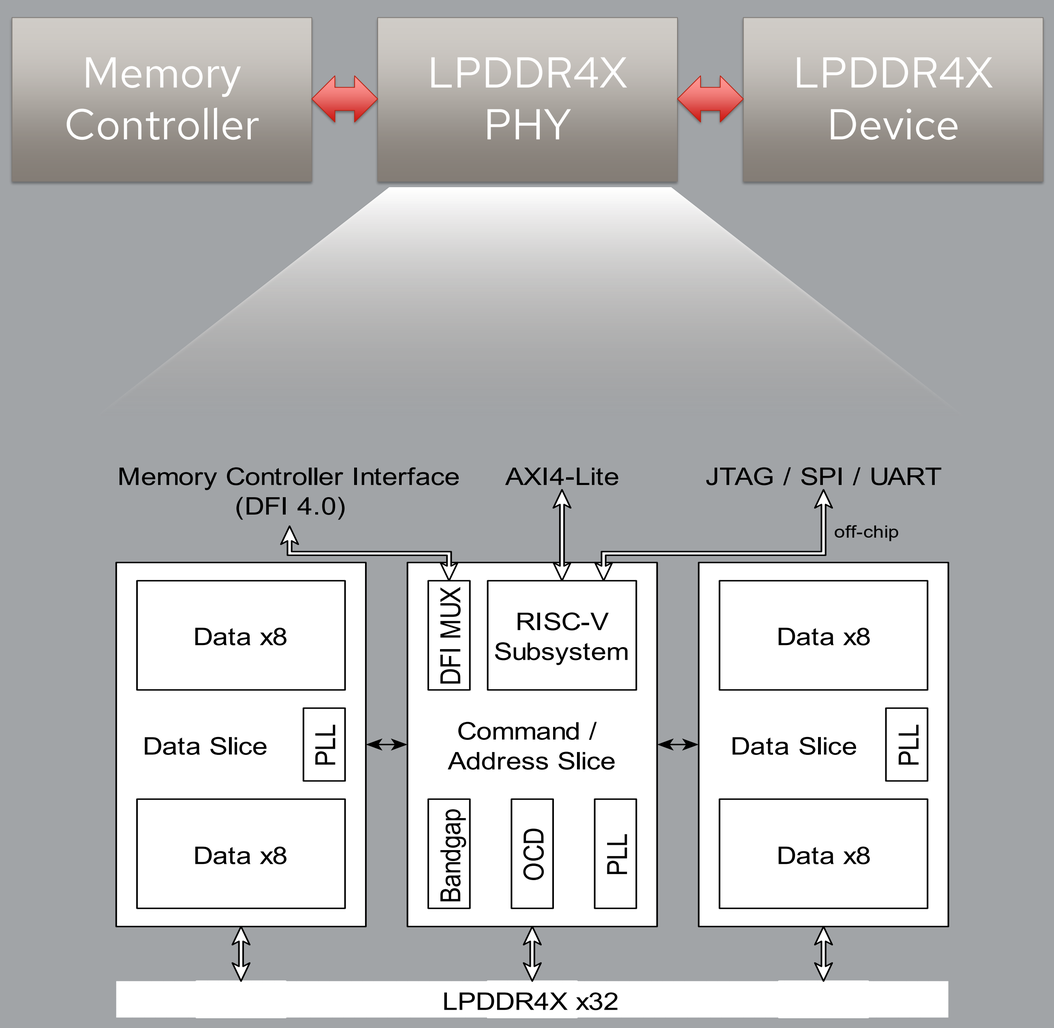
Abstract *- The demand for memory technologies with high bandwidth, low power consumption, and enhanced reliability has led to the emergence of LPDDR4X DRAM memory. However, power efficiency and reliability depend not only on the memory device but also on its interfacing. To enable advanced monitoring of LPDDR4X DRAM devices and interface tuning, we propose a LPDDR4X PHY implemented in 12nm FinFET technology. A RISC-V subsystem offers software-controlled DRAM interface access as well as external interfaces to connect additional sensors for monitoring temperature and current consumption of LPDDR4X DRAM devices.*

We enhance the state-of-the-art PHY architecture with software-controlled low-level DRAM access using a DDR PHY Interface (DFI) Bridge and interfaces for off-chip sensors that are controlled by a RISC-V Subsystem.

In future publications, we will show the impact of this PHY on the overall system power consumption and reliability using the physical chip expected to be delivered in June 2024.

LPDDR4X Architecture



Frequency: 2133 MHz

RISC-V Subsystem Architecture

RISC-V Core

- RV32IMC
- In Order, 3 Stage Pipeline
- JTAG TAP (IEEE 1149.1-2013)

Memory

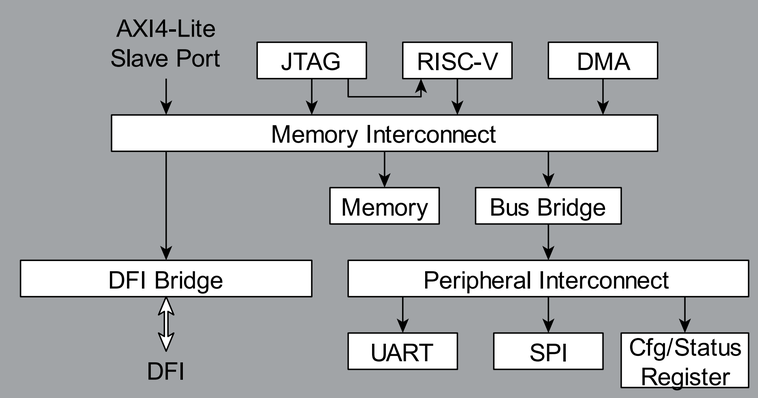
- 64 kB SRAM
- 4 AXI4-Lite Ports

DFI Bridge

- Direct access to DRAM devices
- Calibration / Tuning

Peripherals

- Direct Memory Access (DMA) Controller
- UART
- SPI
- Configuration / Status Registers



Frequency: 1066 MHz (1:2 clock ratio)

Results

Power of RISC-V Subsystem

- 12.6 mW @ 533 MHz
- 24 mW @ 1066 MHz
  → 15% of overall power consumption

Hierarchical Area

- Total PHY Area: 2.89 mm²
- Total area dominated by 150 µm bump pitch

	Cell [µm²]	SRAM [µm²]
RISC-V Subsystem	24468	106641
⊢ **RISC-V**	4518	-
⌞ **DFI Bridge**	4147	48701

DFI Bridge Architecture

DFI Bridge Features

Low-level access to DRAM devices

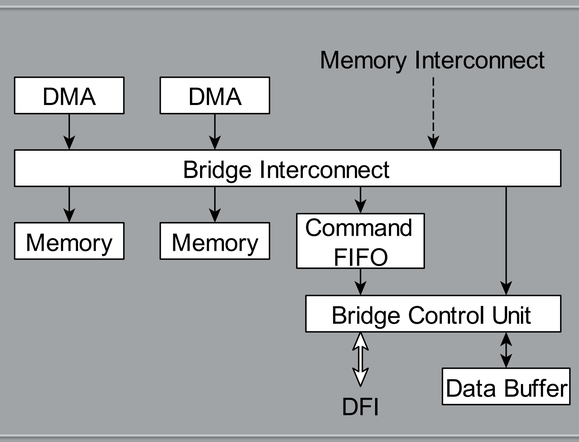
- DRAM initialization
- Benchmarking
- Maintenance

Calibration / Tuning

- Impedance trimming
- WR levelling
- RD calibration / trimming

Architecture

- Bridge Control Unit
- 2x DMA Controller
- 64-bit Interconnect
- 2x 16 KB SRAM
- 256x 512-bit Data Buffer



Command Structure and Features

- 64-bit DFI Command Word
- 2x CA Commands
- Cycle accurate delays
- Index based selection of Write Data
- Automated comparison of Read Data

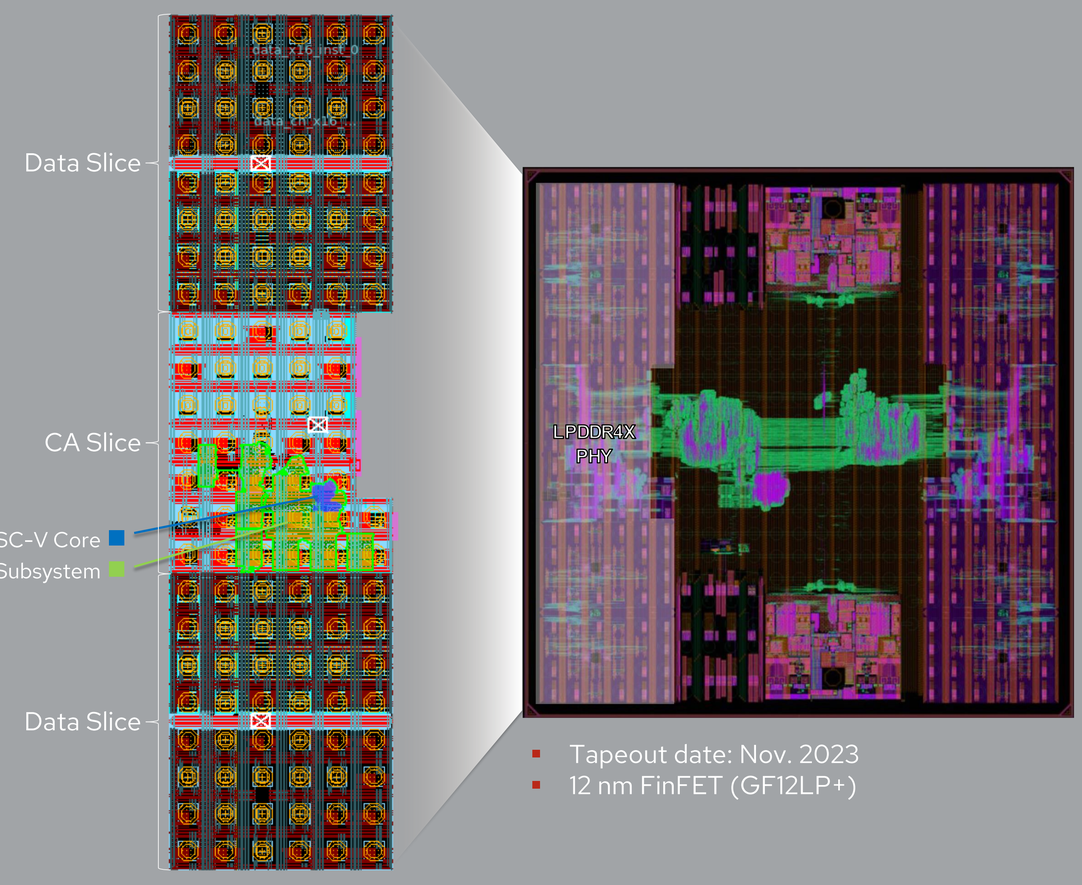
DFI Command

CA Command	CA Command	Address Index	Data Read	Data Compare

CA Command

CA 0	CS 0	CA 1	CS 1	Delay	Data Write

Layout of LPDDR4X PHY



- Tapeout date: Nov. 2023
- 12 nm FinFET (GF12LP+)

RISC-V®

MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

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