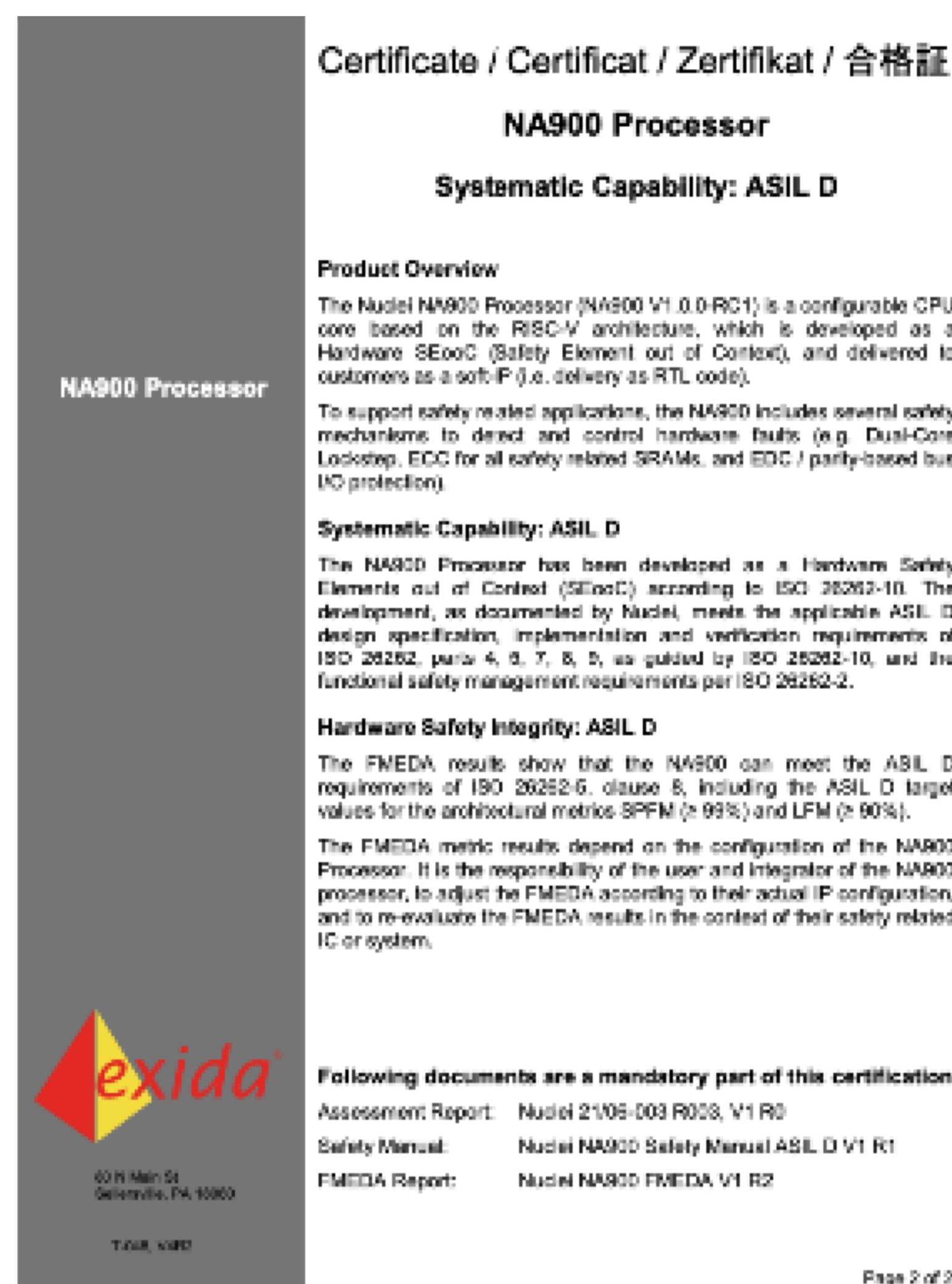
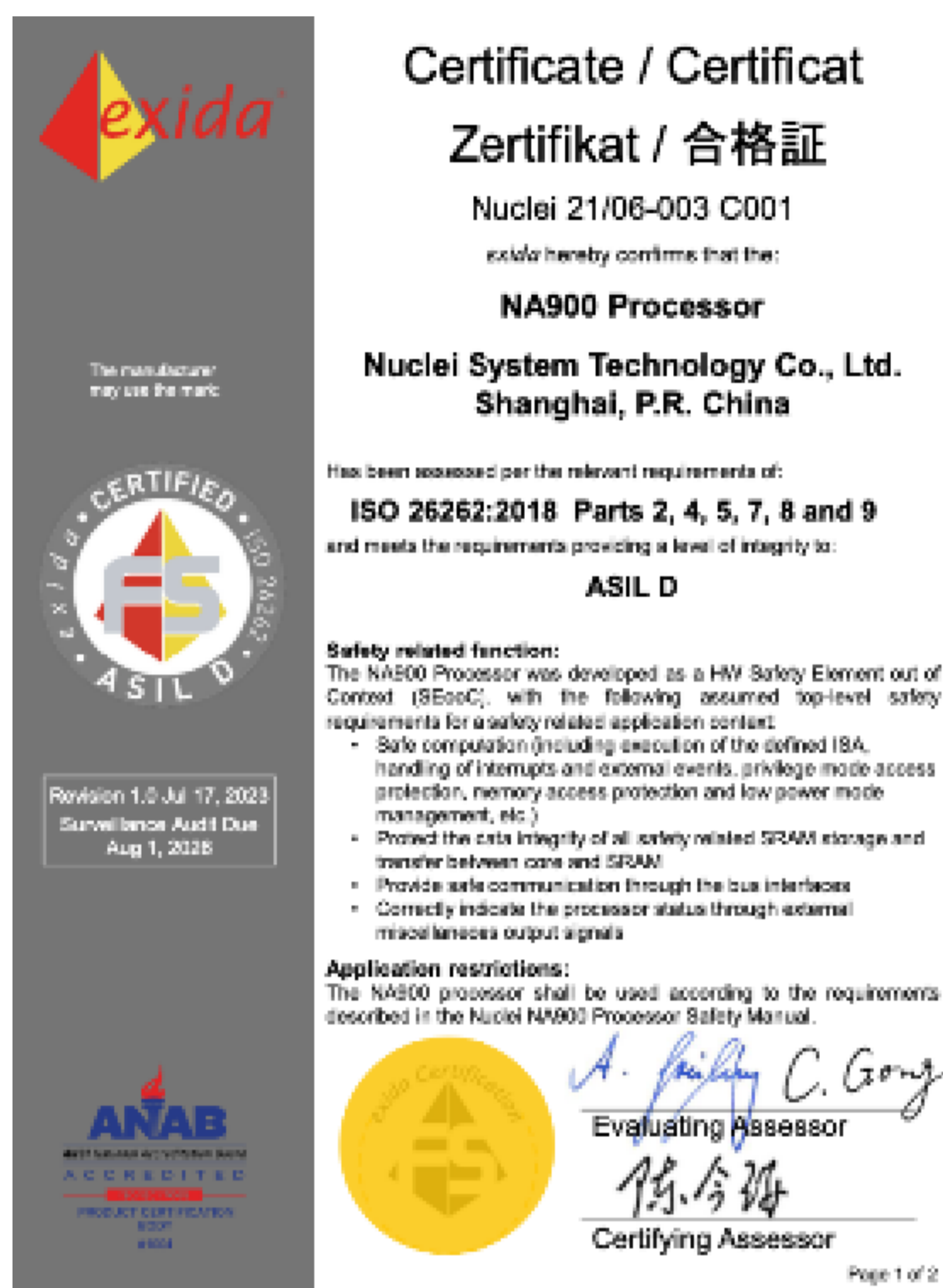


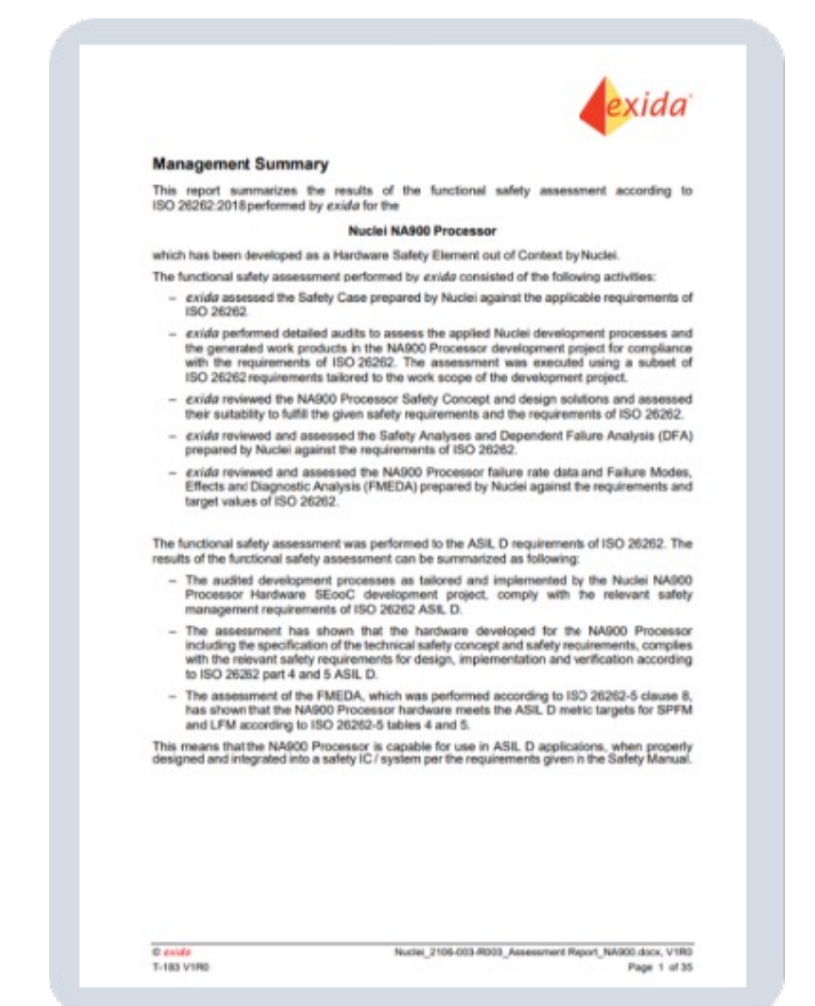
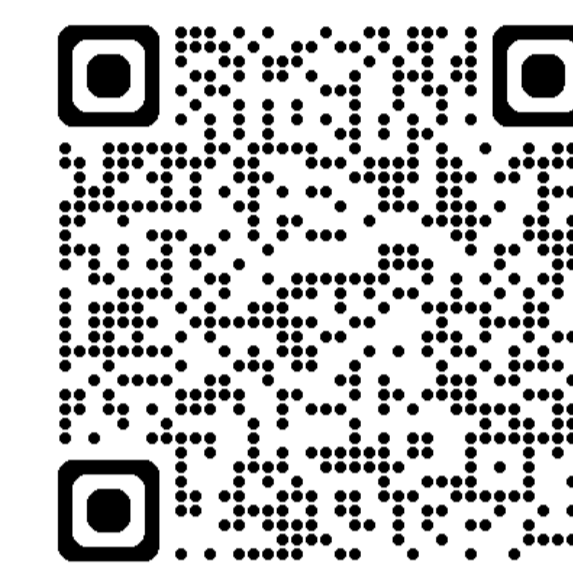
A Leading RISC-V CPU IP and Solution Vendor

NA900-ISO 26262 ASIL-D Product Certified RISC-V CPU IP

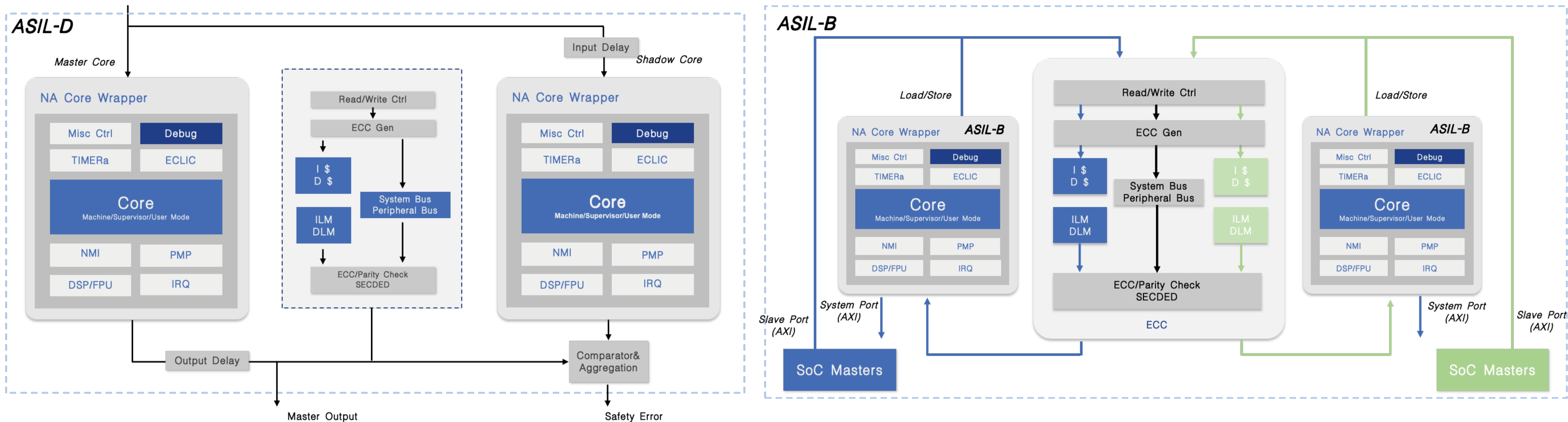


ASIL-D level for Both Systematic Capability and Hardware Safety Integrity

Assessment Report Link



Automotive Application with ASIL-B&D



Safety Package and Real Use Cases

FMEDA							
Block / Subblock [Drop-down]	Block / Component	Block / Component Group	High Level Block / Component Group	Failure Mode (FM) for the block	FM distribution permanent	FM distribution transient	
1	Master core	master core	-	4.7720	All applicable failure mode of computation or communication execution caused by faults in the master core (100) logic	97.0%	99.0%
1	Master core	master core	-	4.7720	Unexpected ECC error detection: 1. Detect error when not expected (false alarm). 2. Not detect & true ECC error.	1.0%	0.5%
1	Master core	master core	-	4.7720	Generate wrong ECC code to the SRAM write data bus	1.1%	1.1%
1	Master core	master core	-	4.7720	Unexpected ECC correction: 1. Do correction on correct data and result in data error. 2. misc & true ECC correction	1.0%	1.0%

Top level safety requirements (TLRS) on IP / IC Level			
TLRS short	SPFM	LFM	
1 NA900 shall provide the required safe computation	99.996%	99.784%	
2 NA900 shall protect the data integrity of all safety related SRAM Storage and transfer between core and SRAM.	99.268%	98.885%	
3 NA900 shall provide safe communication through the bus interfaces	99.996%	99.784%	
4 NA900 shall be configured through external miscellaneous input signals, and correctly indicate the processor status through external miscellaneous output signals.	99.996%	99.784%	

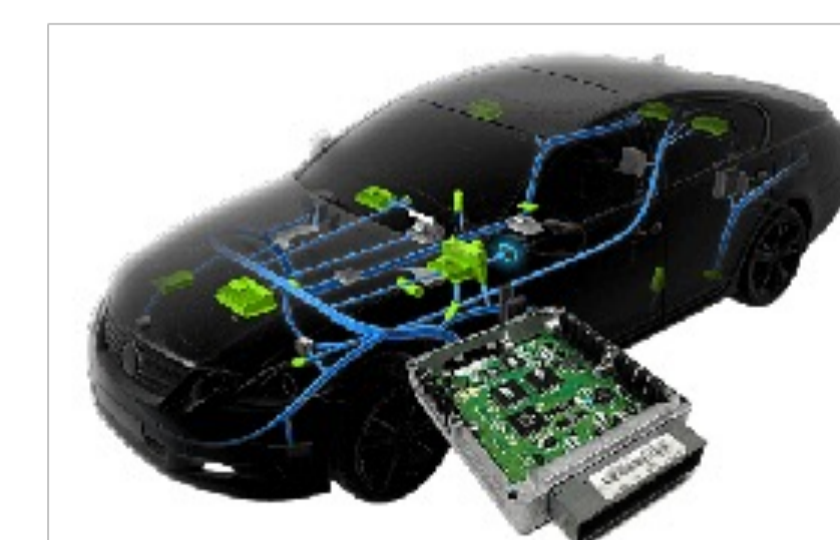
Safety Manual	
2.2. SEoC Overview	<ul style="list-style-type: none"> 2.1.2.1. Definition of Components as SEoC 2.2.2.2. Processor Modes 2.3.2.3. Top-Level Safety Requirements <ul style="list-style-type: none"> 2.3.1.2.3.1. Performance Impact 2.4.2.4. Top-Level Safe States 2.5.2.5. Non-Functional Requirements 2.6.2.6. Constraints and Assumption of Use
3.3. Safety Architecture	<ul style="list-style-type: none"> 3.1.3.1. Safety Status and Fault Signals 3.2.3.2. Safety Measures <ul style="list-style-type: none"> 3.2.1.3.2.1. Detection & Indication and Reaction Time 3.2.2.3.2.2. Internal Safety Mechanism and Design Measures <ul style="list-style-type: none"> 3.2.2.1 3.2.2.1. Safety Measure 1: HWSM-DCLL 3.2.2.2 3.2.2.2. Safety Measure 2: HWSM-SRAM-PROT 3.2.2.3 3.2.2.3. Safety Measure 3: I/O Protection HWSM-I-PROT, HWSM-O-PROT 3.2.2.4 3.2.2.4. Safety Measure 4: Non safety Isolation HWDM-NSI-ISO 3.2.2.5 3.2.2.5. Safety Measure 5: TSC Comparator HWSM-DCLL-TSC 3.2.3.2.3. External Safety Mechanism <ul style="list-style-type: none"> 3.2.3.1 3.2.3.1. Safety Measure 6: Watchdog Timer HWSM-EXT-WDG 3.2.3.2 3.2.3.2. Safety Measure 7: External Check on Protected Output Signal HWSM-EXT-O-CHECK 3.3.3.3. Assumption of Use for Safety Mechanisms
4.4. Integration Requirements	<ul style="list-style-type: none"> 4.1.4.1. IP configuration 4.2.4.2. Configuration Parameters 4.3.4.3. External Hardware Blocks 4.4.4.4. Verification Activities of Integrator 4.5.4.5. Additional Support From Nuclei



Lidar ASIL-B



Gateway ASIL-D



Domain Controller ASIL-D



ADAS ASIL-D

Contact: neil@nucleisys.com