北京开源芯片研究院
BEIJING INSTITUTE OF OPEN SOURCE CHIP

RISC-V at BOSC: Achievements and Challenges

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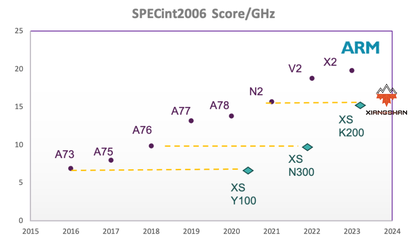
BOSC Introduction

Missions

Misson 1: Develop open-source & high-performance RISC-V CPUs ---- Xiangshan CPU family.

Misson 2: Build-up open-source RISC-V ecosystem.
· Development infrastructure & tools
· Chip design methodologies: open-source verification & Agile(a.k.a Minjin) development flow



Partnership & Cooperation

Ecosystem Partner

International cooperation of RISC-V

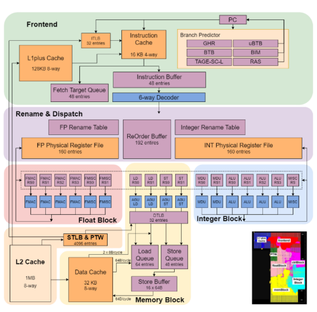
BOSC is deeply involved in community organizations such as the RISC-V International , and becoming its Premier member as well as a member of the RISE Foundation. It is also a member of OpenHW and a partner of embedded world China, and is actively partici-pating in the strategic planning and technical route formulation of international RISC-V open source organizations.

Premier member of RISC-V International | Member of the RISE Foundation | Member of OpenHW | Partner of embedded world China

Achievements

Xiangshan CPU Family

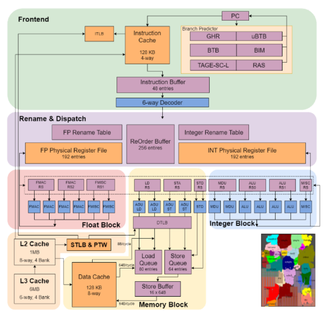
2021 XS Y100



1.3 GHz @ 28nm, 7.01/GHz

EOL

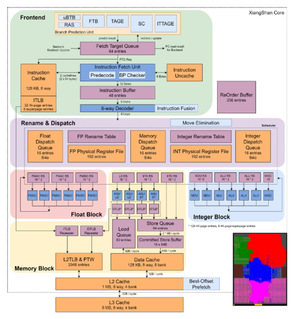
2022 XS N300



2.1GHz @ 14nm, 9.55/GHz

Balanced Perf & Efficiency
(v.s. ARM A76)

2024 XS K200



3GHz @ 7nm, 15/GHz

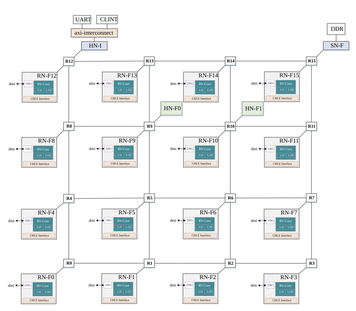
Ultimate Performance
(v.s. ARM N2)

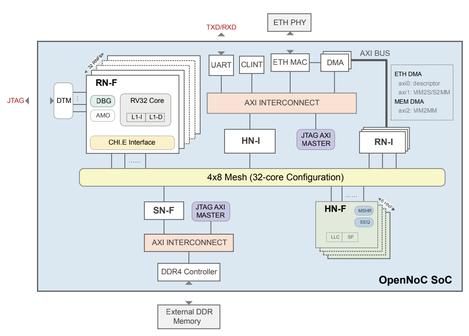
Xiangshan CPU Feature List

Feature	YQH	NH	KMH
Pipeline depth	12	12	12
Rename width	4	4	6
ROB size	192	192	256+
ALUs	4	4	4
L1 instr cache	16KB	64KB	64KB
L1 data cache	32KB	64KB	64KB
L2 cache	1024KB	256KB	1024KB
L3 cache	NA	Up to 4MB	Up to 16MB
NoC support	N	N	WIP
ITLB	32	32	48
DTLB	32	128 direct mapped	48
L2 TLB	2048	2048	2048
Vector	N	Y	Y
Virtualization	N	N	Y
ECC support	N	Y	Y
PMA/PMP support	N	Y	Y
Debug support	N	Y	Y
External interface	AXI4	AXI4	AXI4/CHI
ISA	RV64GC	RV64GCBKV	RV64GCBKVH
Frequency@Process	1.3GHz@28nm	2GHz@14nm	3GHz@7nm
SPECint 2k6	7/ GHz	10/ GHz	15/ GHz

Open Network-on-Chip

·ARM AMBA 5 CHI 0050E.b
·MESI based Cache coherency
·Use Non-inclusive, Non-Exclusive policy
·Support SF (Snoop Filter), maximum size 8MB
·Support end-to-end QoS（Quality of Service）
·Up to 8×8 Mesh
·Up to 128 RN-F nodes
·Up to 16 NH-F nodes, with each HN-F's LLC size ranging from 0 t0 32MB
·Up to 32 DDR channel
·256-bit data channel





Challenges

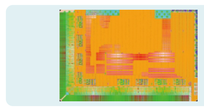
Challenge 1: CPU Development Flow

Traditional hardware development flow:
· Long development cycle: ~1.5 -2 years
· High cost: involves hundreds of engineers
· Lengthy debug/verification infrastructure
· Self-maintained/developed infra/platform

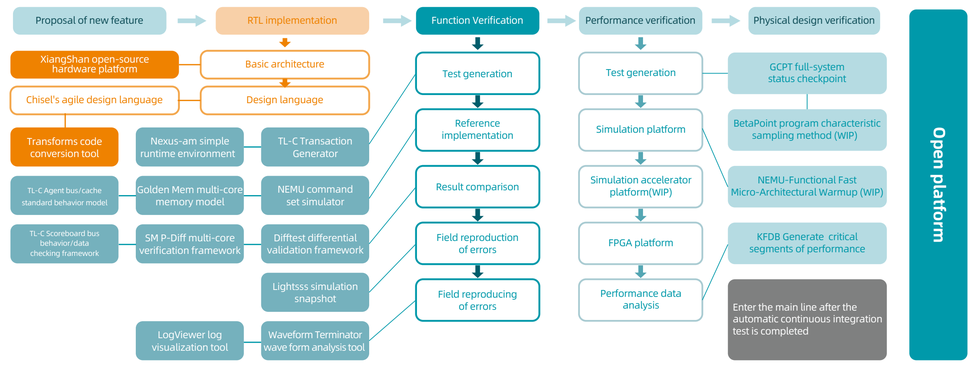
Innovation

Agile development flow:
· In-house developed infrastructure -- Difftest
· Over 20 proprietary tools for testing
· One of the 12 Top Picks in Architecture in IEEE Micro 2022

Agile Infrastructure



Open-source design

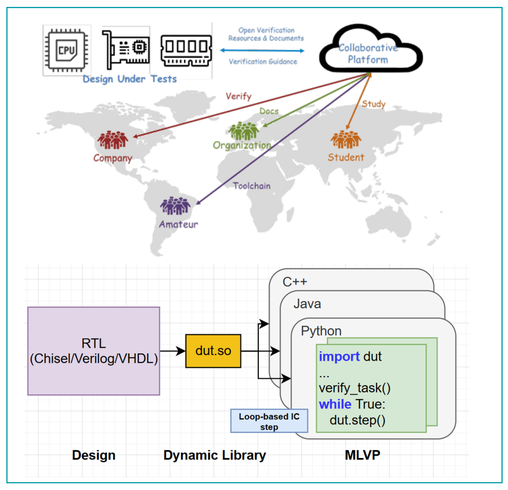


Challenge 2: Verification

Traditional verification:
· High expense: verification engineers >= design engineers
· Language barrier: RTL expert
· Non-uniformed infrastructure or platform

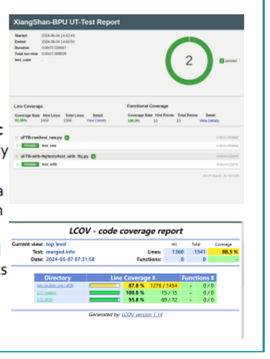
Innovation

UnityChip verification:
· Standard & free verification platform
· Test cases using high-level languages (e.g. python) or RTL
· Multi-language support



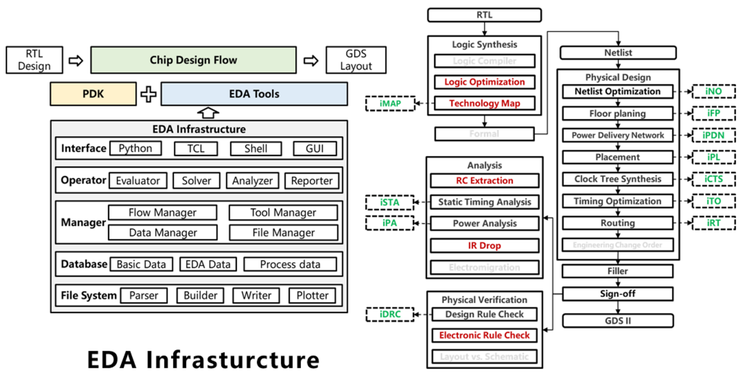
Case Study

- We have used **UnityChip** to verify the **branch predictor unit** submodule in the front end of the Xiangshan Kunminghu processor. During the verification process, we divided the module into six subtasks: uFTB, Tage-SC, FTB, ITTAGE, RAS, and BPU Top.
- We have collected verification data such as **code coverage** and **functional coverage**. We can also **map** this coverage **data to specific lines** of code to selectively improve them.
- Five undergrads utilized a **pytest-based** verification **environment** which identified some bugs and **achieved** coverage results **comparable to** those of **traditional** verification teams.



Challenge 3: Hardware Design EDA Tools

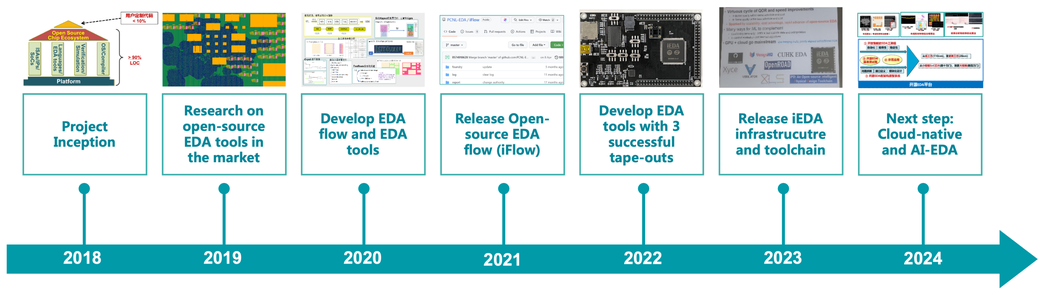
iEDA is an open-source digital chip design platform.



EDA Infrasturcture

11 Tools

iEDA Milestones



For Your Information

https://www.bosc.ac.cn
https://open-verify.cc/en
https://github.com/OpenXiangShan
https://Xiangshan-doc.readthedocs.io

BOSC Wechat Official | Xiangshan Wechat Official | iEDA Git Wechat Official | UnityChip Verification | Xiangshan Git Repo | iEDA Git Repo