Utilize Sampling and Calibrated Microarchitectural Simulator to Boost Hardware/Software Co-design of Xiangshan Processor

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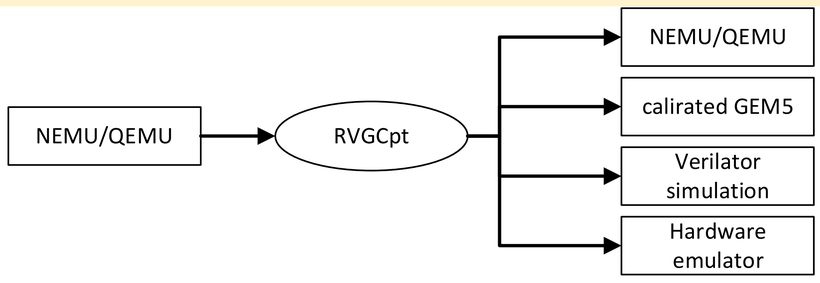
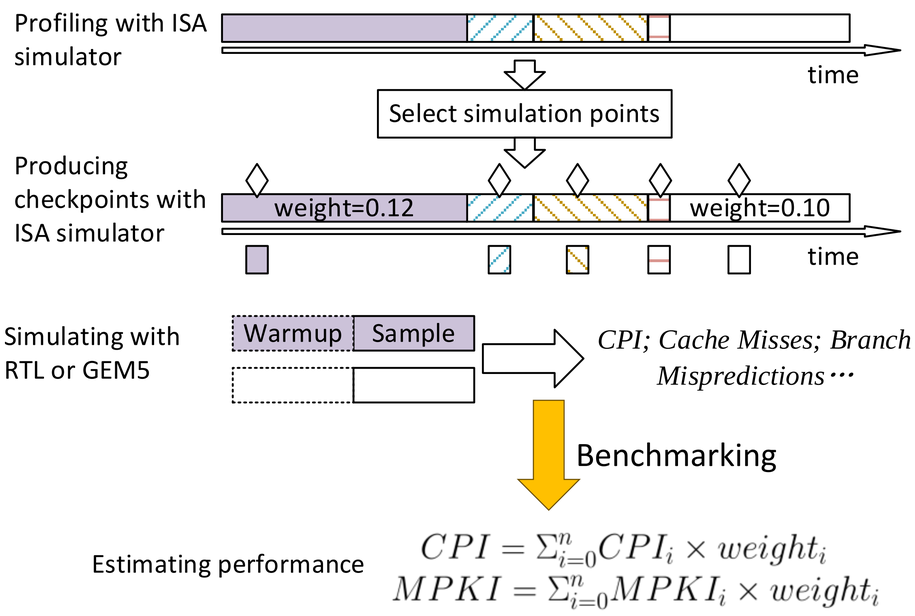
- **One** checkpoint for **four platforms**

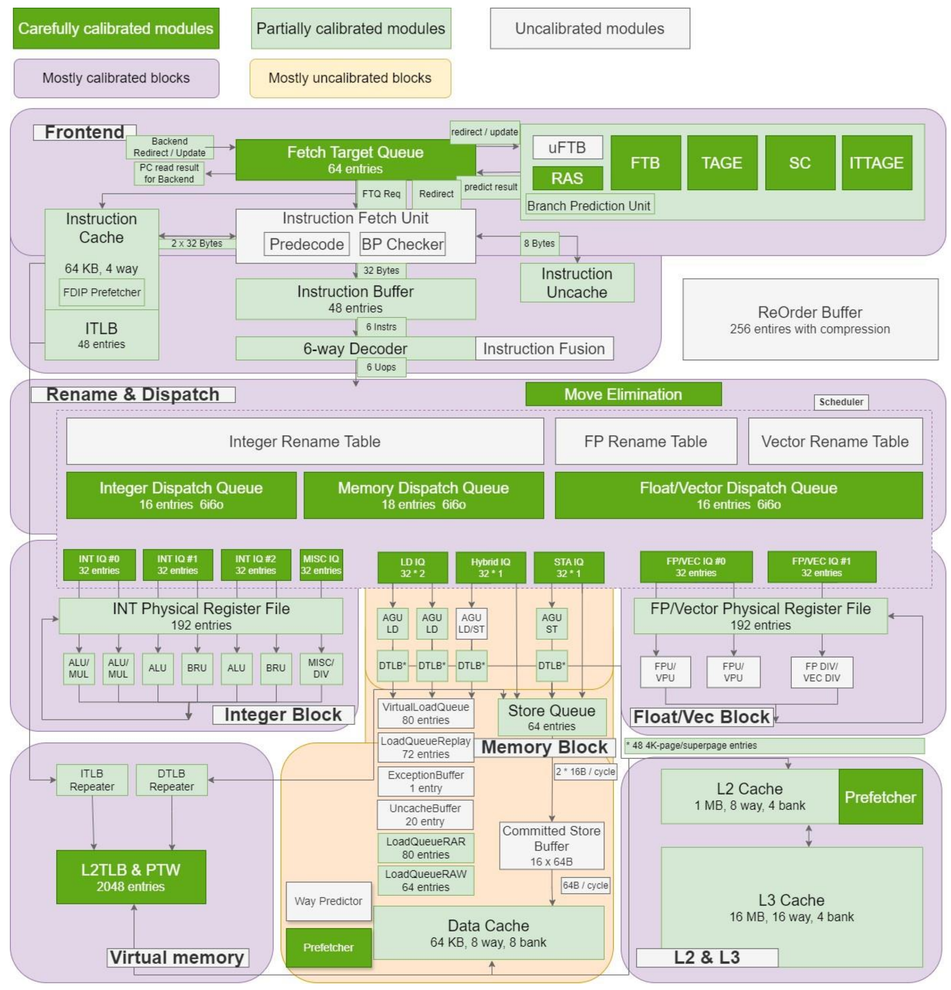


- Checkpoints for benchmarking & Calibrating



Calibrating

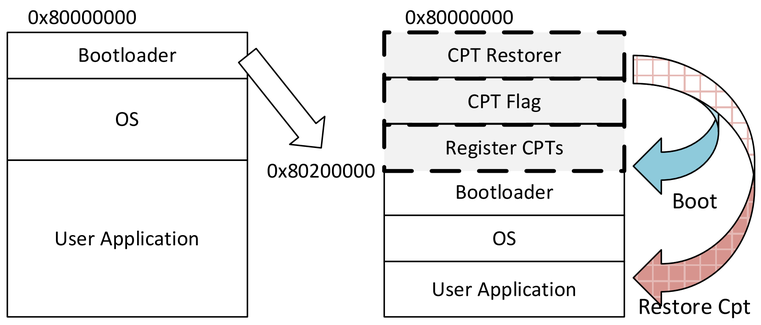
- Calibrated simulator (GEM5): **SPECint2k6 = 45@3GHz**



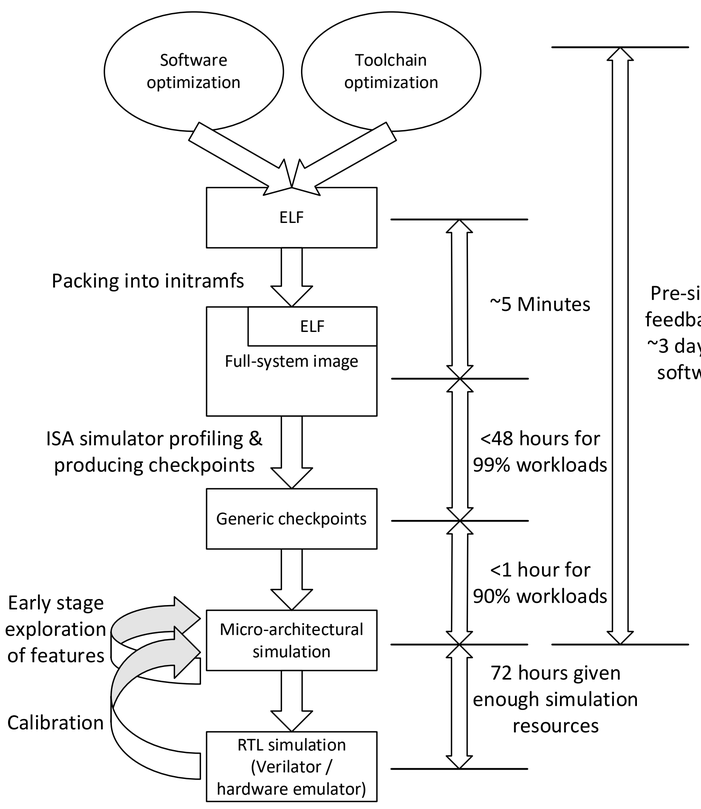
Checkpoints and workflows

- Generic checkpoint format easy to integrate into simulator/RTL in early stages
- Pre-silicon Hw/Sw codesign with both simulator and RTL feedback
- Correlation against full workloads on FPGA and real silicon

- Pure software-based cpt restoring



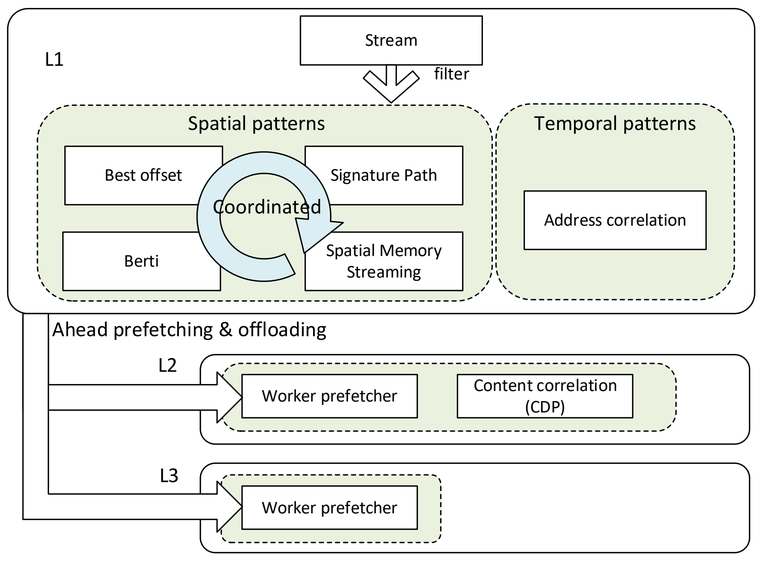
- Early-stage performance feedback for Hw/Sw co-design



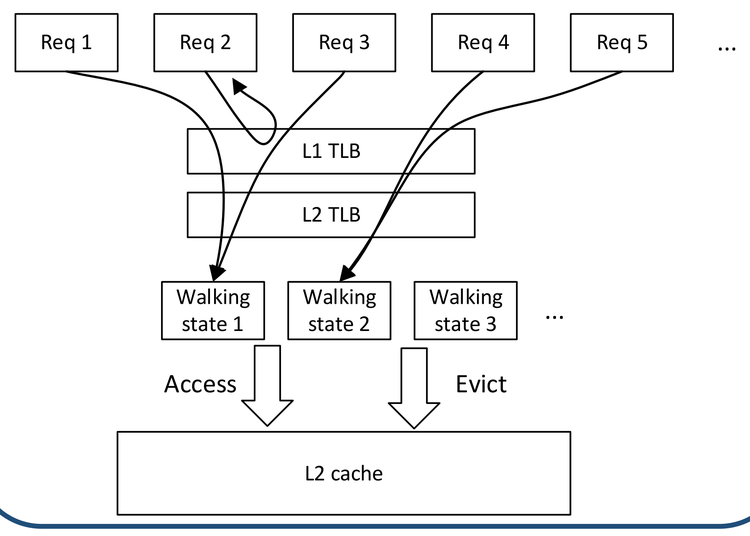
Microarchitecture

- Estimated **SPECint2k6 score = 45@3GHz**
- Top-down counters and analysis suite
- Multi-level TLBs and parallel coalescing PTW with RV-H extension
- Tightly-coordinated composite prefetcher with mutual parameter updating, cooperated training, and flexible offloading
- Decoupled frontend 3-level branch predictors
- Distributed backend with 2x128 bit OoO vector pipeline

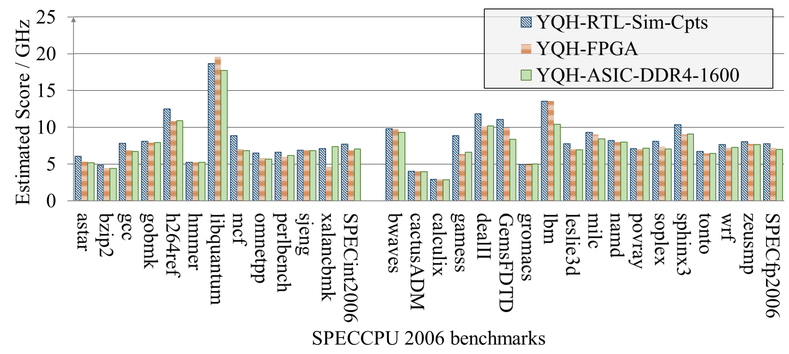
- Tightly-coordinated composite prefetcher



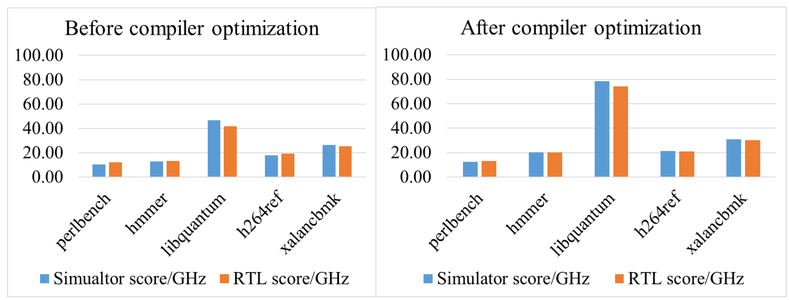
- Parallel Page Table Walking with Coalescing



- Checkpoint performance is highly-correlated with full workloads



- **Pre-silicon Hw/Sw co-design** with Microarchitectural Simulator



Simulator repo:
https://github.com/OpenXiangShan/GEM5

My Homepage:
https://shinezyy.github.io/ArchShineZ/

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