CHERI RISC-V: A Case Study on the CVA6

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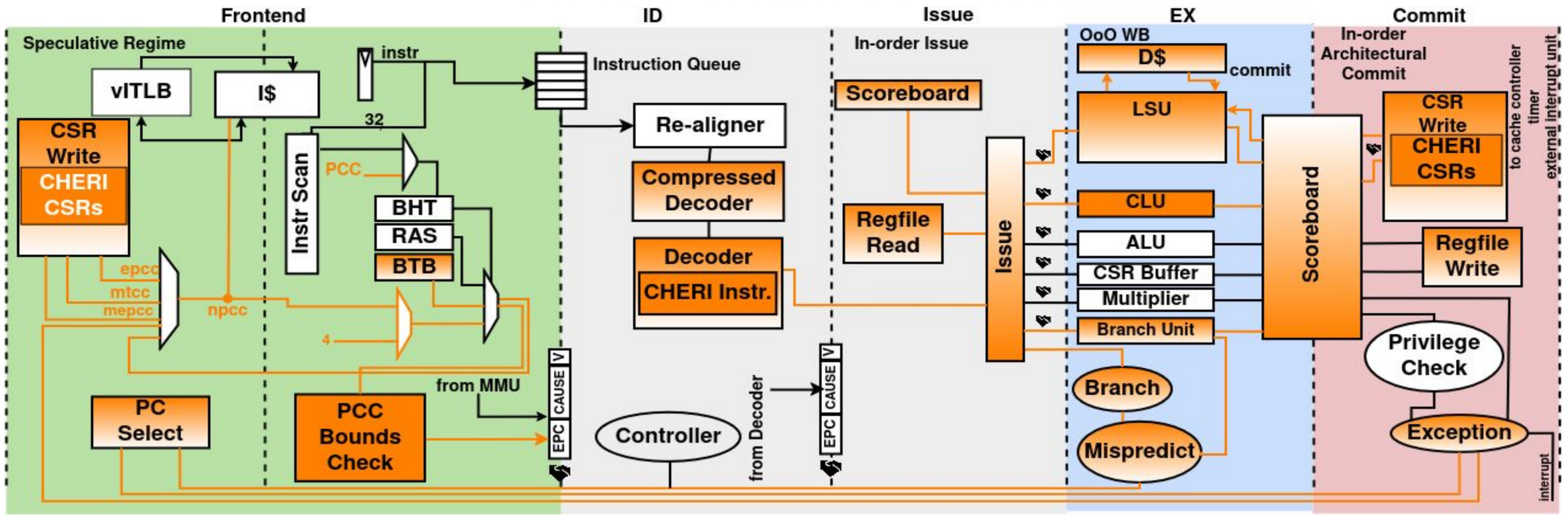
Abstract

We report our work on extending the open-source RISC-V CVA6 with CHERI support. Our implementation complies with version 9 of the CHERI RISC-V specification. Currently, we are evaluating and validating our design in an experimental single-core system-on-chip (SoC) in a simulation and FPGA emulation environment. To our knowledge, this will be the first public RISC-V CPU with hardware virtualization and CHERI support. We plan to release our CVA6H-CHERI core as an open-source artifact to the RISC-V and CHERI community.

CVA6H-CHERI Overview



Features and Status

- RISC-V CHERI ISA v9 Cambridge
- RV64 (MMU and MMU-less)
- Merged Capability Register File
- Supports Integer and Capability mode
- Hybrid and Pure Capability Code
- Optional extension
- Tagged-memory support
- Compressed Capability Format CHERI-128
- CHERI SCRs
- Capability-Manipulation Instructions
- CHERI & Hypervisor extension
  - Hyp SCRs (vstcc, vsepcc, vstdc)
  - Hypervisor Load/Store Cap. Instructions (hlv/hls)

Validation

- **TestBenchs Simulation** (Done)
  - Unit Tests Cheri Logic Unit, Branch Unit, and Load/Store Unit
- **FPGA Emulation** (Done)
  - Experimental SoC with Tagged Memory support
- **Baremetal Tests** (WiP)
  - Handwritten C Tests built atop the riscv-hyp-bare
- **TestRig** (WiP)
  - CVA6 RVFI-DII Support (Done)
  - Top-level Verilator model (WiP)
- **Bao Hypervisor** (WiP)
  - Started porting Bao hypervisor to CHERI using QEMU
- **CheriBSD** (WiP)

Hardware Resources

Module	Resource	Utilization
cva6 SoC	LUT	**101587** (+36%)
	FF	**56107** (+33%)
cva6	LUT	**68991** (+38%)
	FF	**26284** (+31%)
wt_cache_subsystem	LUT	**9963** (+23%)
	FF	**3034** (+36%)
cheri unit	LUTs	**1953** (1.9%)
tag controller	LUTs	**6662** (6.6%)
	FFs	**6165** (10%)

Post-synthesis hardware utilization results for single core CVA6H-CHERI SoC targeting a Genesys 2 FPGA with TagController.

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