From ISA to Industry: Accelerating Technical Progress and RISC-V adoption in 2025

Andrea Gallo

13th May 2025

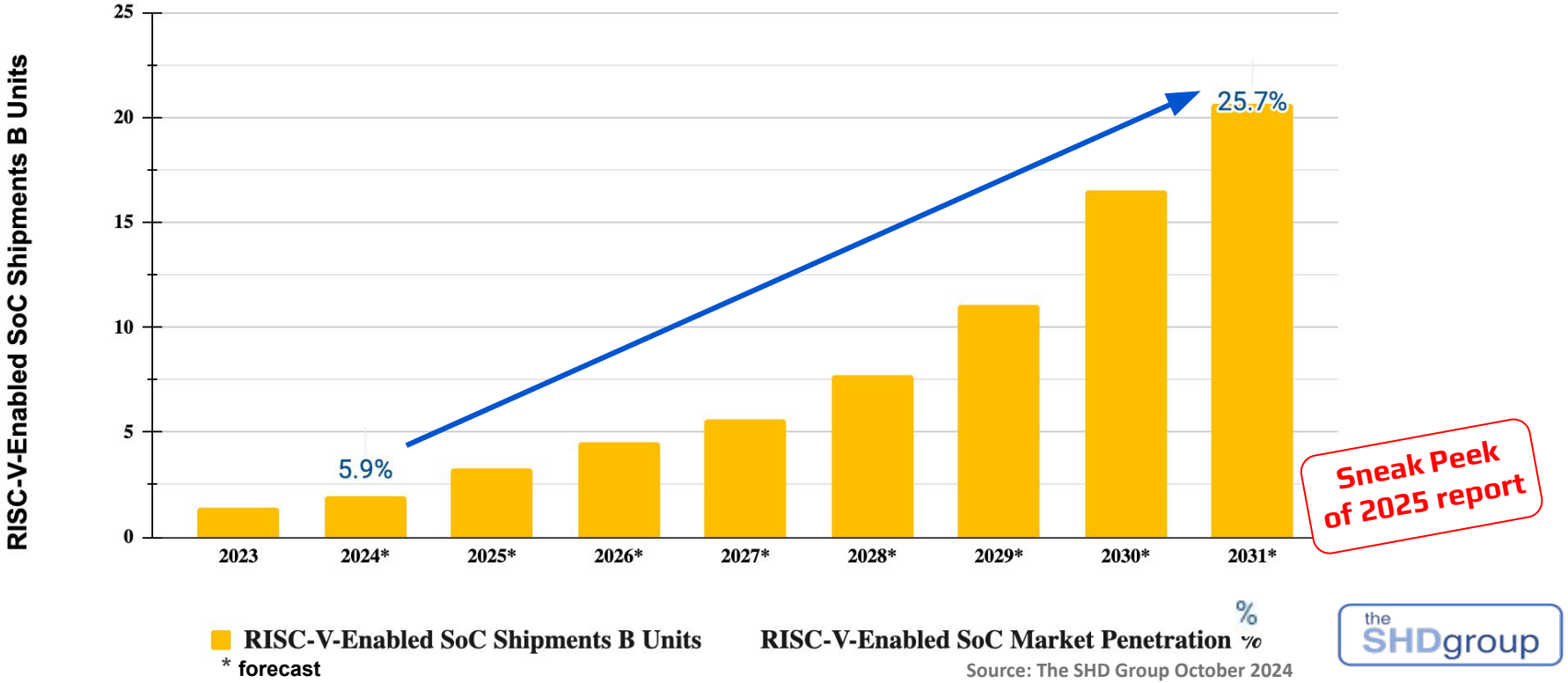
“RISC-V Poised for a Big 2025”

“RISC-V’s success has extended beyond embedded computing to storage technology and HPC, demonstrating the architecture’s broad momentum”

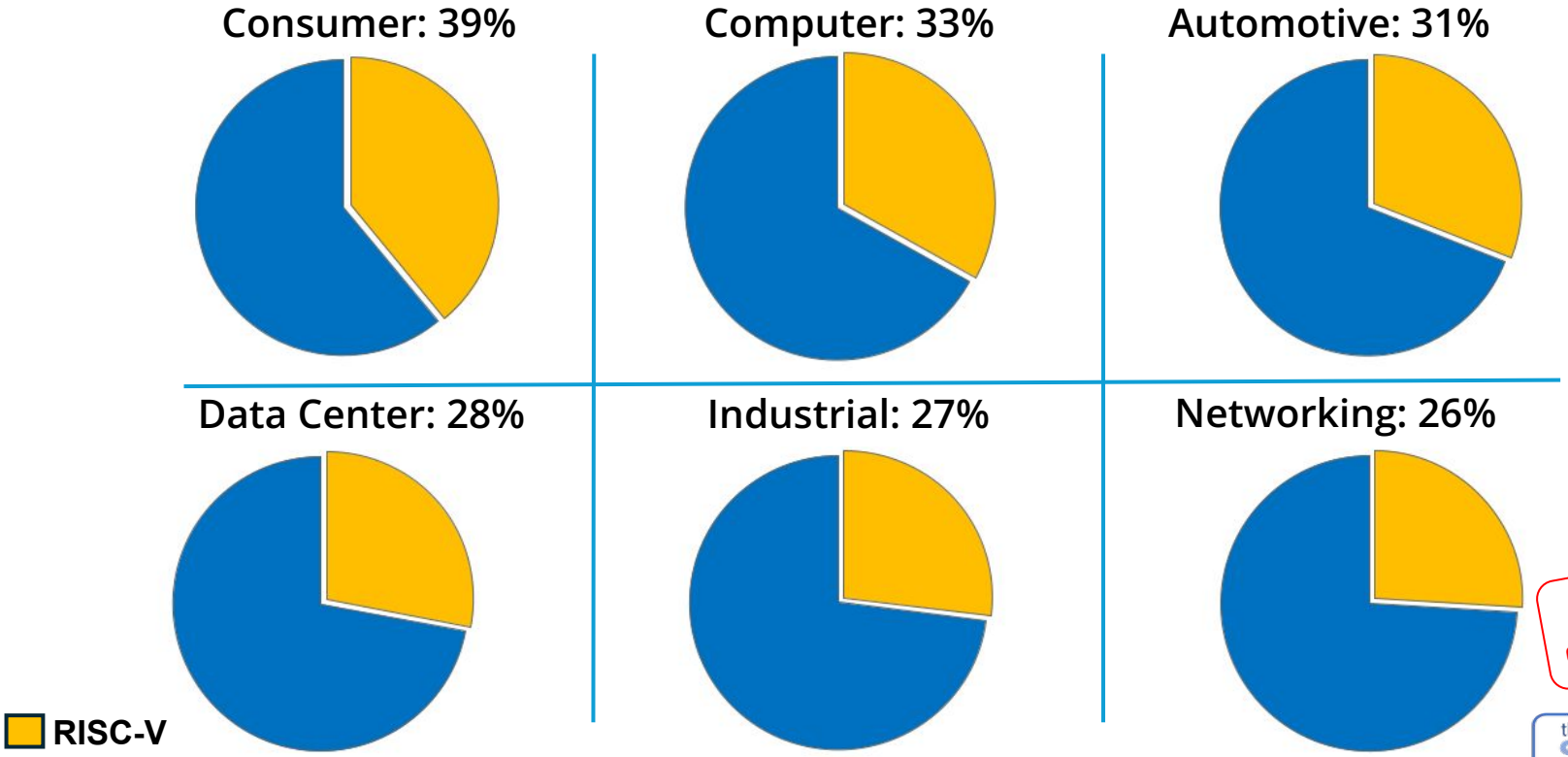
Source: Embedded Processor Architectures
VDC Research, April 2025

RISC-V®

20B RISC-V SoCs, to Surpass 25% of Market



Top Markets for RISC-V 2031

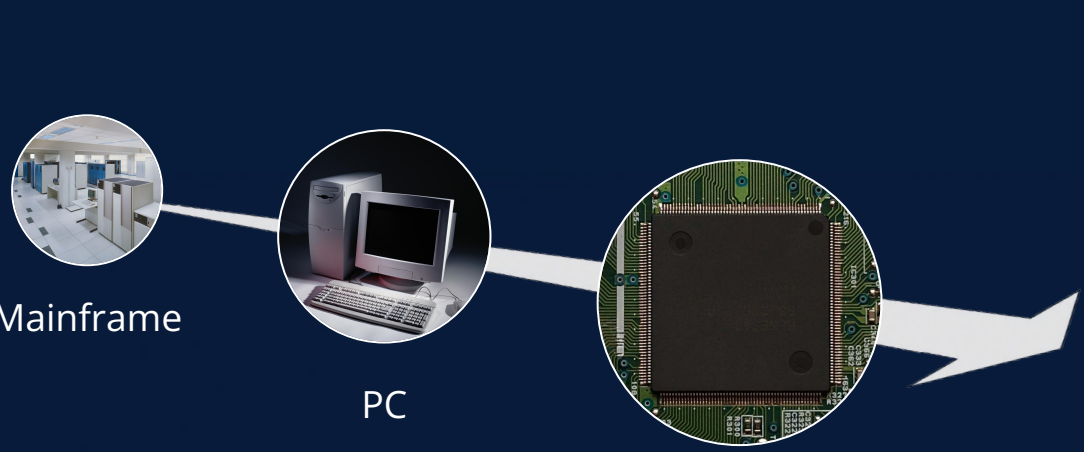


Sneak Peek of 2025 report

the SHDgroup

Source: The SHD Group October 2024

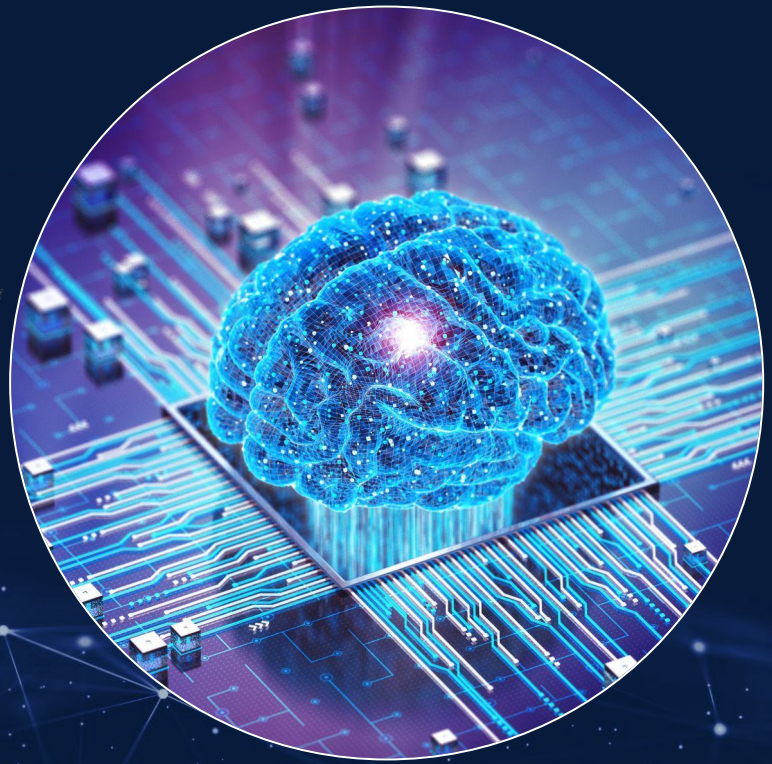
Delivering a new era of Workload-designed Silicon



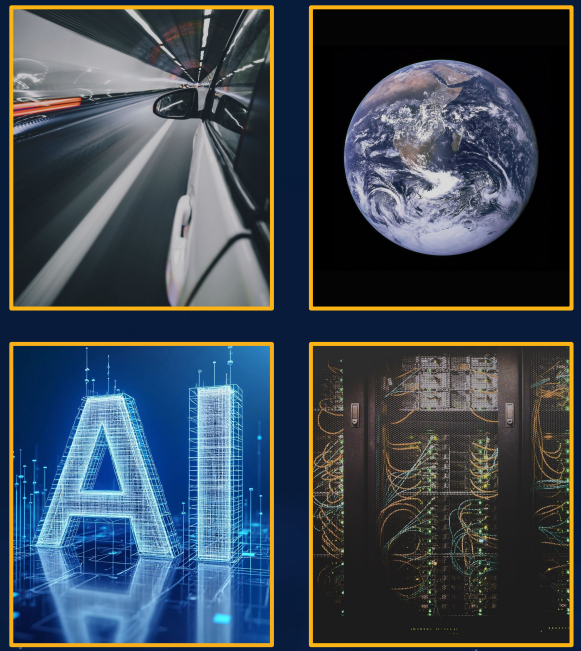
Mainframe

PC

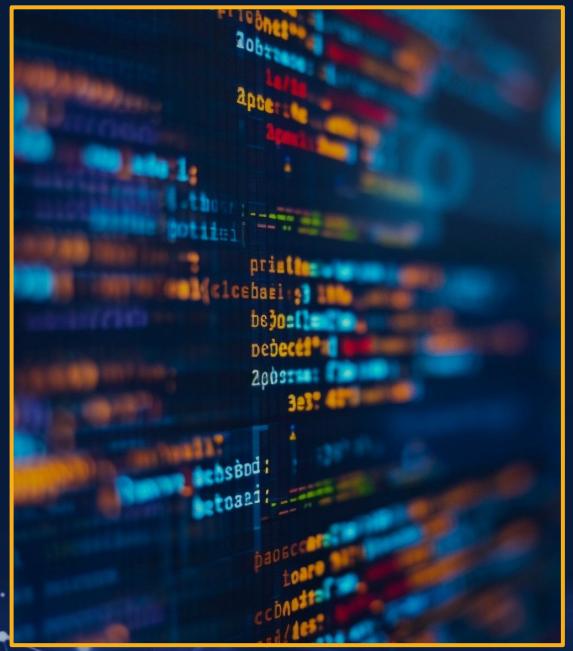
SoC



RISC-V®



Prioritize Industry Verticals



Focus on Developer Experience

RISC-V®

Industries

Automotive

Infineon announces the introduction of an automotive RISC-V microcontroller family

Cortus MINERVA Out-of-Order 4GHz 64-bit RISC-V Processor Platform targets automotive applications

MIPS releases P8700 CPU targeting driver assistance and autonomous vehicle applications

Andes Technology D45-SE Processor Achieves ISO 26262 ASIL-D Certification for Functional Safety

PLS add support for the RISC-V ISA to test and debug Infineon automotive processor design

HighTec EDV-Systeme GmbH has added support for Nuclei System Technology's RISC-V CPU IP

Automotive SIG

Advocates for automotive in Technical Groups and SIGs

Maintains a "gap analysis"

Interfaces with industry initiatives

Investigates AI for automotive applications

Development of RISC-V auto technologies

Develops ecosystem support

Panel – Accelerating Automotive Innovation with RISC-V: The journey from early adoption to industry wide deployment

Wed 14 at 17:15

Chips JU and the Vehicle of the Future – a RISC V view

Georgi Kuzmanov, Chips JU. Wed 14 at 16:30

Data Center

Rivos and Canonical partner to deliver scalable RISC-V solutions in data centers

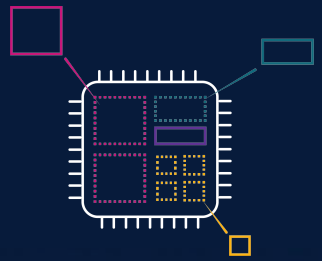
Alibaba launches RISC-V-based XuanTie C930 server CPU built for AI-HPC workloads

RISC-V Koji instance is now live in Fedora data center

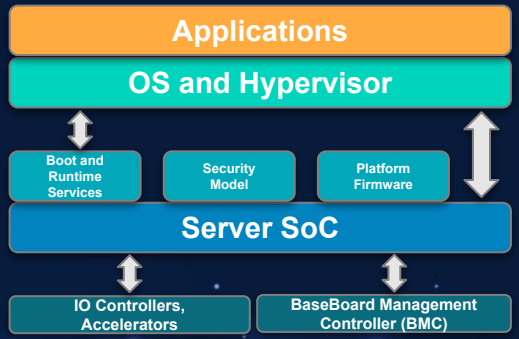
SpacemiT Develops Server CPU Chip V100 for Next-Gen AI Applications

Ventana Veyron V2 high performance data center-class RISC-V processor and platform

Server SoC - Standardizes the requirements for the hardware interfaces and capabilities provided by the SoC



Server Platform - A standard set of capabilities, encompassing areas where divergence is typically necessary across implementations



Cloud based RISC-V servers: How and why we built them, how you can use them

Fabien Piuzzi, Scaleway. Wed 14 at 10:00

Artificial Intelligence

Andes Technology demo its RISC-V IP in a Spherical Image Processor and Meta's AI Accelerator

Nvidia shipped over 1 Billion RISC-V processors in 2024

Ubitium debuts universal RISC-V processor to enable AI

AheadComputing secures $21.5M to drive RISC-V innovation for AI and cloud

Semidynamics launches a RISC-V SDK with ONNX Runtime support

Axelera AI secures up to €61.6M grant to develop scalable AI chiplet for High-Performance Computing

AI / ML Special Interest Groups

Explore new data formats and algorithms vs vector and matrix extensions

Evaluate best integration options for AI Software frameworks

Space

Frontgrade Gaisler launches new GRAIN line and wins SNSA contract to commercialize first energy-efficient neuromorphic AI for space applicationsa

UK defence contractor BAE Systems is using a security digital twin of a RISC-V processor from SiFive for a radiation hardened chip for space

Microchip unveils 64-bit HPSC Microprocessor (MPU) family for autonomous space computing

ESA and NASA both using RISC-V for space computing

Space SIG

Understand space requirements

Advocate for space in Technical Groups and SIGs

Maintains a “gap analysis”

Investigate AI and HPSC

Leading edge security capabilities

Develops ecosystem support

RISC-V: Reaching New Orbits in Space Computing

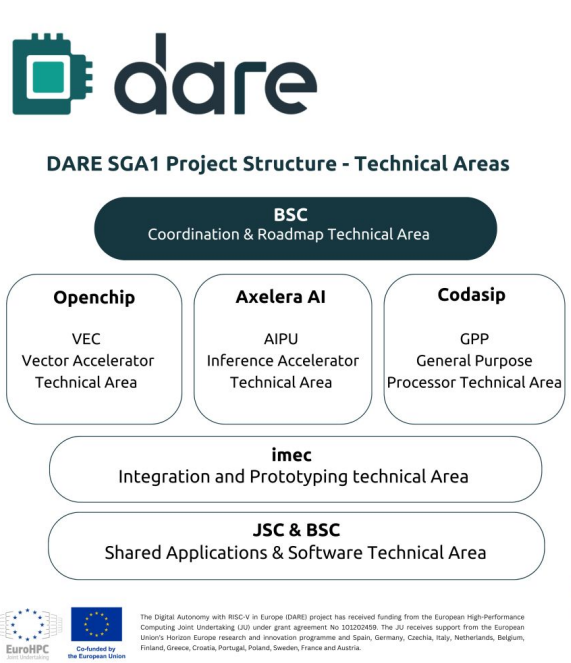
Lucana Santos, ESA. Thu 15 at 11:30

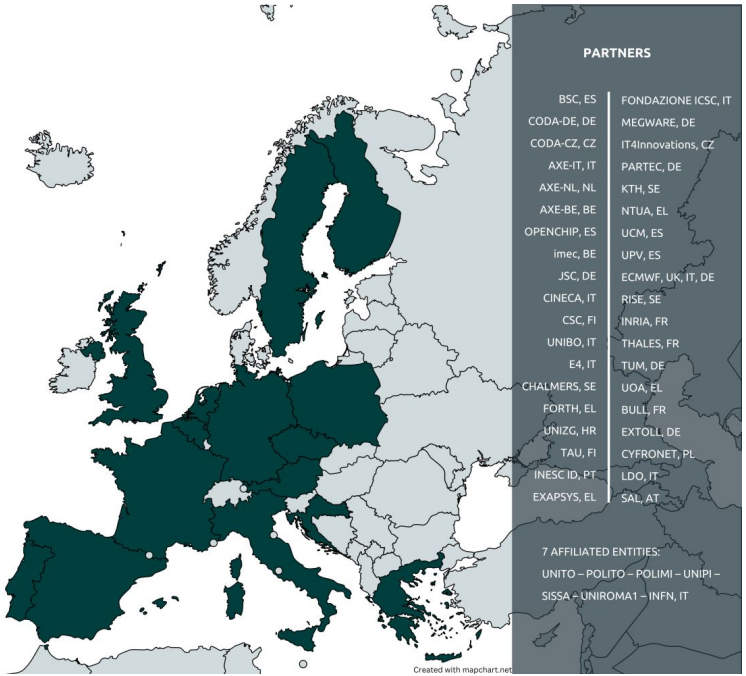
HPC

Baya Systems and Semidynamics collaborate to accelerate RISC-V system-on-chip development

Openchip, NEC and Barcelona Supercomputing Center studying collaboration to develop next generation supercomputers based on RISC-V

Esperanto Technologies and NEC cooperate on initiative to advance next generation RISC-V Chips and software solutions for HPC





RISC-V: Powering the Future of HPC?

Nick Brown, EPCC. Wed 14 at 14:30

From Open Silicon to Sovereign Supercomputing

Alexandra Kourfali, EuroHPC. Wed 14 at 14:45

Membership

Peter Schiefer

Division President &
CEO Automotive

Infineon Technologies

ESWIN

Ning He

CTO

ESWIN Computing

New Strategic Members

mobileye™

SCI Semiconductor

TRUSTONIC

CloudBEAR

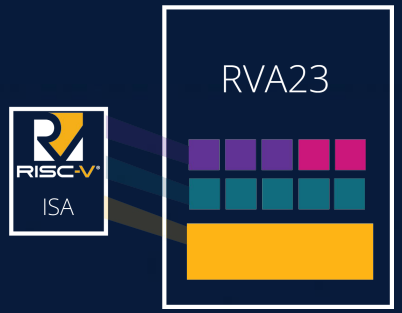
igalia

芯朋 Chipown
High Performance Power Semiconductor

MOORES LAB AI

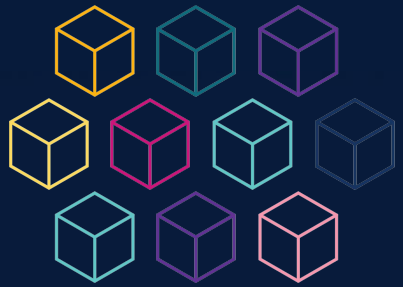
Developer Experience

RVA23

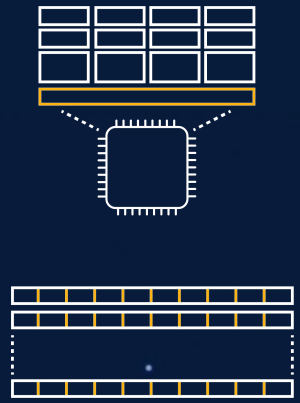


RVA23 specifies a set of mandatory and optional features, providing a common target for developers

RVA23 underwent a lengthy development, review, and approval process



Profiles enable a large application and systems software ecosystem.



Key components of RVA23 include the Vector and Hypervisor extensions

Enabling Developers with Hardware

- 280 boards shipped in 2024
- Current boards
  - Banana Pi F3
  - SiFive Premiere P550
  - Milk-V Megrez
- Boards sent to multiple open source community projects
- Reach out to RISC-V International to participate in the program

10x ENGINEERS

PLCT Lab

epcc

RISC-V Online Learning

https://riscv.org/certifications-and-courses/

Barna Ibrahim

Vice-Chair

RISE

RISC-V®

Collaborating more closely than ever before

- Compilers
- Toolchains
- System libraries
- Kernel
- Virtualization
- Programming languages
- Linux distribution integration
- Tools for debug and profiling
- AI/ML

+


yocto
PROJECT
RISC-V®
+
RISE
RISC-V Software Ecosystem
RISC-V®

Josef Holzmayr
Community Manager
The Yocto Project

RISC-V®

- Official RISC-V Yocto Images
- Full positive test coverage will be required before release
- Long Term Support (LTS) releases for 4 years
- Support for all RISC-V profiles
- RISC-V representative on Governing Board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Have an amazing RISC-V Summit Europe 2025!