High Performance RISC-V Processor for Application in Harsh Environments

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Abstract

This work introduces a full custom RISC-V processor specifically targeted for harsh environments capable of sustained operation at 180 MHz while withstanding temperatures up to 175°C. Built using a state-of-the-art 180nm silicon-on-insulator (SOI) technology, the processor overcomes the limitations of existing designs, such as increased leakage currents and reduced carrier mobility in extreme environments. Key innovations include a deeply pipelined architecture optimized for thermal stability, modular execution pipelines to handle high-latency operations without stalling, and tightly coupled caches using single-port SRAM with custom wrappers for high throughput. In contrast to other well known architectures for harsh environments, which usually target radiation resistance in space, this design is tailored specifically for high-temperature resilience. Extensive testing validated its performance and reliability.

Introduction

The increasing demand for high throughput digital signal processing in extreme environments, such as those found in aerospace, space exploration, and industrial applications, requires processors that can operate reliably under varying temperature effects. Traditional processor architectures and designs often fail to meet the stringent requirements of these applications due to performance degradation and reliability issues at elevated temperatures[1]. Off-the-shelf RISC-V designs, such as PULP [2], while effective in many contexts, are constrained by the limitations of their underlying technology nodes. For example, when implemented on a 180nm process [3], the PULP platform reaches frequencies around 40MHz due to the limitations required to protect the design from high temperatures and additional design constraints [4, 5].

Other architectures such as LEON using the SPARC Instruction Set Architecture (ISA) [6], are tailored for space applications and optimized for radiation resistance and low-temperature environments. This is in contrast to the high-temperature demands of this work, making them less suited for operation at sustained temperatures of up to 175°C. For example, conventional CMOS-based designs suffer from increased leakage currents and reduced carrier mobility under high temperature effects, leading to significant performance degradation. These limitations highlight the need for architectures that are inherently more robust and adaptable to extreme environmental conditions. This processor is designed for application in the high temperature environment of deep drilling.

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Design Challenges and Innovations

Designing a processor capable of such performance under extreme thermal conditions required overcoming key challenges in pipeline design, memory architecture, and thermal management. Several concepts were implemented and elaborated to achieve these goals.

Reliability and thermal management were integral to the design. The processor utilizes a state-of-the-art 180nm silicon-on-insulator (SOI) technology node specifically designed to withstand extreme temperatures. This technology employs high-temperature interconnects, thermal stress mitigation layers, and enhanced oxide layers to ensure reliable operation at sustained temperatures of up to 175°C. The processor incorporates fault-tolerant features, including error detection and correction mechanisms, to mitigate the effects of prolonged operation in extreme conditions. In current work additional dynamic voltage scaling shows further enhances reliability by reducing power consumption and thermal output during operation.

The processor itself uses a deeply pipelined architecture to maximize throughput and mitigate performance bottlenecks. This is mainly done by maintaining consistent instruction throughput, the deeply pipelined architecture addresses the challenges aforementioned induced by the harsh environment. Advanced prefetching mechanisms have been integrated into the Instruction Fetch Unit (IFU) to maintain a consistent instruction supply and minimize stalls. A hybrid branch prediction strategy further reduces the impact of control flow changes, ensuring efficient operation even in high-stress scenarios [4]. This combination of pipeline depth and intelligent instruction manage-

ment is critical to achieving both high performance and thermal stability.

To address the latency disparity between different instruction types, a modular execution pipeline design has been implemented. Depending on the complexity of each operation different pipeline length are implemented: high-latency operations such as division are assigned extended pipelines, while simpler operations such as additions and memory loads use shorter pipelines. This modular design prevents congestion, optimizes resource use, and maintains efficient throughput under heavy workloads.

The design distributes workloads across multiple stages to reduce thermal hot spots and ensure stable operation at 175°C. Out-of-order write-backs help mask delays from long execution units, improving overall throughput. Unlike complex out-of-order issue designs, this approach preserves a simplified architecture optimized for high-temperature performance. Additionally, the deep pipeline design minimizes clock skew-related degradation, critical in extreme environments.

The memory subsystem was another area of focus, using tightly coupled caches built on single-access SRAM for their superior speed and thermal tolerance. A custom wrapper emulates dual-port behavior, since only single port SRAM blocks were able to reach the desired clock frequencies. This allows the system to handle simultaneous reads and writes while retaining the clock frequency of single-access designs. As detailed in the work by Frühauf et al. [7], this approach significantly reduces design complexity and power consumption compared to true dual-port memory, while achieving comparable performance for typical workloads. The wrapper intelligently schedules memory access requests to avoid contention, ensuring minimal latency impact even during high-frequency operations. This approach minimizes memory latency and supports the high-frequency demands of the processor. Prefetching mechanisms further enhance memory efficiency, particularly for linear instruction streams common in embedded applications.

Results and Contributions

This new RISC-V can sustain operating frequencies of over 100MHz at 175°C, with peak performance of up to 180MHz in gate-level netlist simulations; initial measurements of the fabricated chip so far show peak performance of 280MHz at room temperature.Using high branch prediction accuracy, significantly reducing pipeline stalls increasing the IPC up to 0.8 [4]. This processor is able to calculate a window 16 FFT using floating point values in 1.62ms. All these guarantees reliable performance in high thermal environments, validated by extensive stress testing in gate-level-netlist simulations. Further results are currently gathered using the fabricated chip.

Conclusion

This work presents a new RISC-V processor designed for harsh environments that achieves high performance and reliability at extreme temperatures. The adapted in pipeline design, memory architecture, and thermal resilience demonstrated in this processor set the stage for future advances in high temperature disgital singal processing as an on the edge technolgy. By leveraging the modularity and adaptability of the RISC-V ISA, this work provides a robust foundation for the development of processors tailored for mission-critical applications in the aerospace, energy, and industrial sectors.

This processor uses the RISC-V architecture, being full ISA compliant and opens up new possibilities for computing in previously inaccessible environments. Future work can build on this work, exploring improvements in power efficiency, scalability, and integration with specialized workloads to further extend the reach of high-temperature computing using RISC-V processors.

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