IMS
Institute of Microelectronic Systems
Architectures and Systems Group

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Leibniz Universität Hannover

A RISC-V Processor Architecture for Harsh Environments

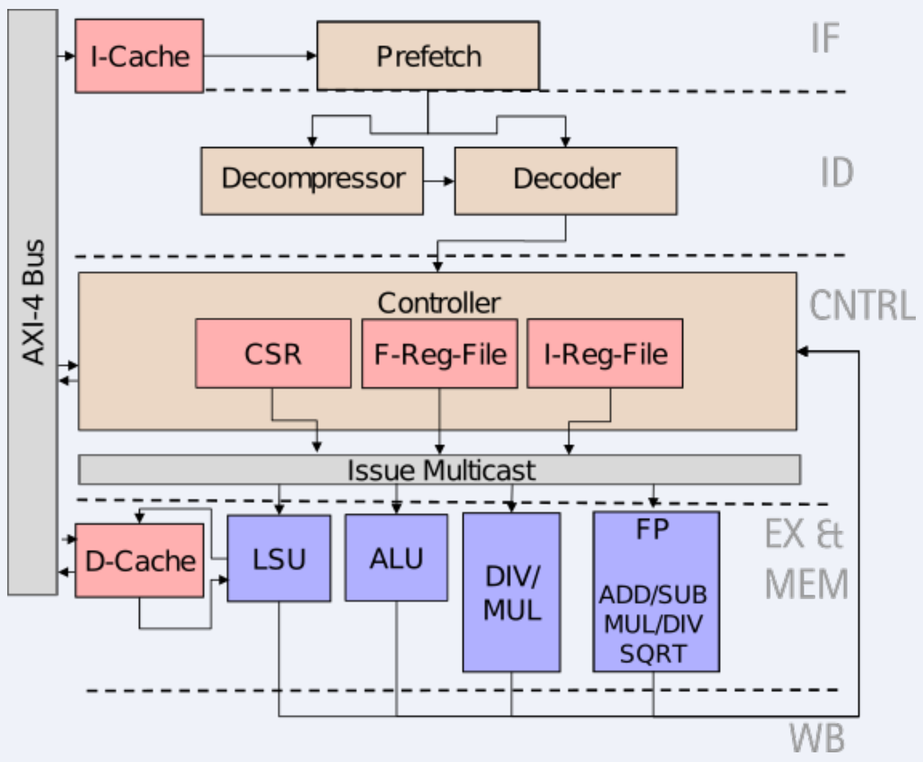
Malte Hawich[1], Malte Rücker[2], Tobias Stuckenberg[2] and Holger Blume[1]

[1]Gottfried Wilhelm Leibniz University Hanover – Institute of Microelectronic Systems
[2]Drilling Services, Baker Hughes, Celle

Motivation & Objectives

- Designed for harsh environments like deep drilling, space, and industrial edge computing.
- Commercial processors fail at sustained high temperatures (>150 °C), limiting performance.
- Need for high-throughput, reliable, and thermally robust CPUs at up to 175 °C.

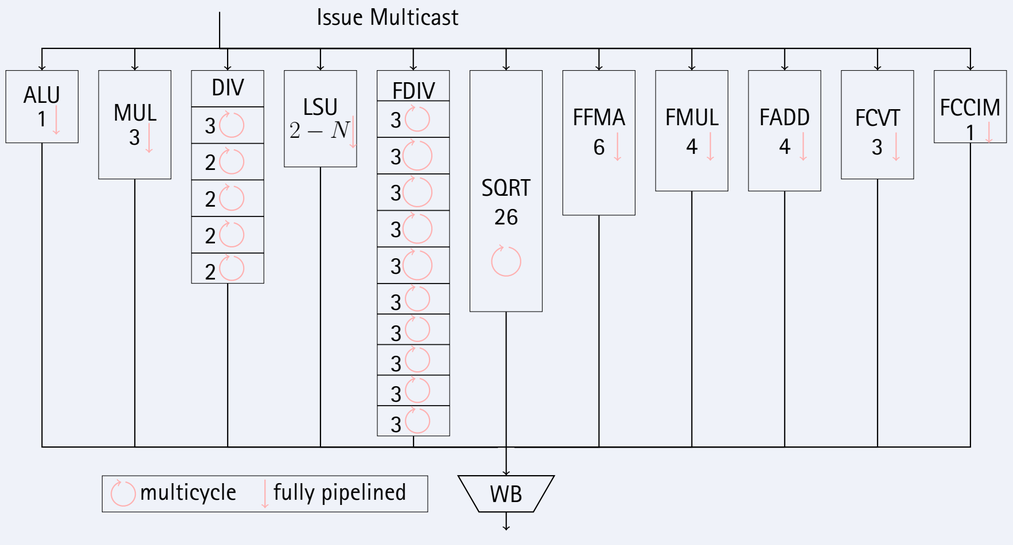
RISC-V Processor Architecture



Key Technical Highlights

- RISC-V processor with RV32IMC or RV32IMFC instruction set
- Fabricated in X-FAB XT018 180 nm SOI – optimized for high-temp
- Peak frequency: 170 MHz
- Innovative out-of-order write-back (OoW) without OoO issue logic
- Deep prefetch-based instruction fetch mitigates slow SRAM latency
- Deep Pipeline (1 to 30 cycles for execution units)
- Robust hazard detection and bypassing, enabling high IPC

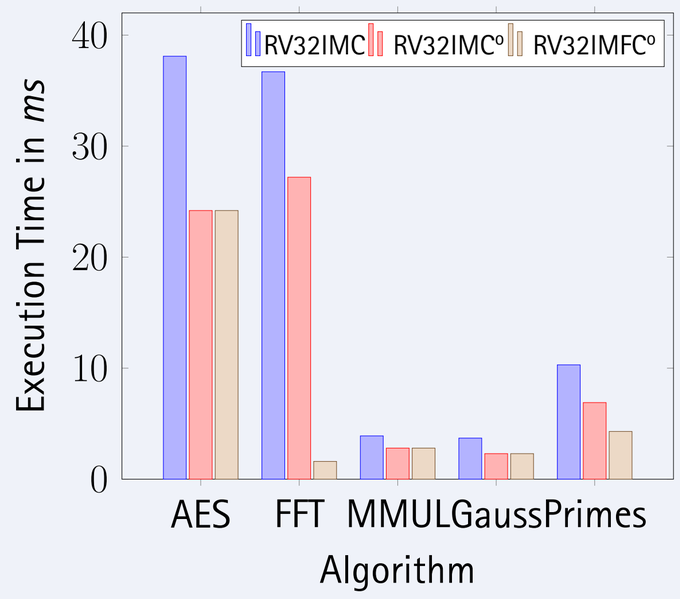
Execution Units



Execution Pipeline

- Instruction dependend pipeline depth (1 to 30 cycles)
- Control overhead offloading using AXI-Stream style handshake mechanism for execution units – controller communcation
- In-Order Issue, Out-of-Order Write-Back
- Latency hiding of slow multicycle units possible if the unit is not needed for the next instruction

Results



- Significant performance improvement with OoO write-back
- Floating point unit benefits from OoO write-back

Area, frequency, power consumption and CoreMark performance of the different processor versions

	fully in-order			out-of-order write back	
	RV32I	RV32IC	RV32IMC	RV32IMC⁰	RV32IMFC⁰
Area in mm^2	2.10	2.11	2.50	2.24	3.62
Max Freq. in MHz	160	160	142	170	170
Power in mW	130	132	159	171	356
CoreMark/MHz	0.50	0.50	1.36	1.44	-

CoreMark performance comparison:

- RV32IMC⁰: 244.8 CoreMark with 1.44 CoreMark/MHz at 170 MHz
- Ibex (build in the same tech node as our core) : 118.9 CoreMark with 3.13 CoreMark/MHz at 38 MHz
- Commercial Vorago (Hardsil®): 116.5 CoreMark with 2.33 CoreMark/MHz at 50 MHz

Literature

[1] M. Hawich, N. Rumpeltin, M. Rücker, T. Stuckenberg, H. Blume, "High performance instruction fetch structure within a risc-v processor for use in harsh environments", *International Conference on Embedded Computer Systems*, 2023

[2] M. Hawich, J. Szücs, H. Blume, "High temperature in-order risc-v processor with heterogeneous pipeline and out-of-order write-back mechanism", *Kleinheubach Conference* 2024

[3] 0.18 Micron Modular BCD-on-SOI Technology. *XFAB Manual, X-FAB Silicon Foundries* 2020