Enabling Front-End SoC Integration Automation Flows for Large RISC-V Designs

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Context

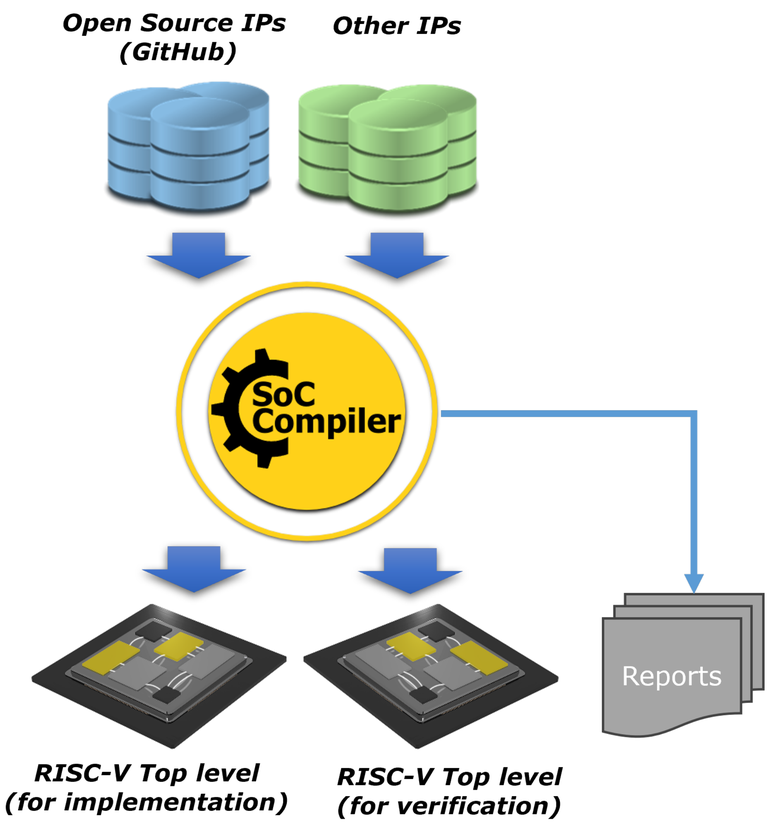
- RISC-V based designs are becoming increasingly complex
- Traditional SoC design process involves: IP selection, configuration, connection, file generation, and validation
- SoC designers need automated solutions to shorten Turn Around Time
- Current solutions often rely on custom scripts that aren't easily reusable between projects

Problem Statement

- Manual RTL design processes are time-consuming and prone to human errors
- Errors typically appear late in design cycles, consuming valuable project time
- Custom scripts lack portability between different design projects
- Design restructuring to meet physical constraints requires multiple iterations
- Hierarchy changes affect logical descriptions and require extensive verification

Methodology: A New Design Platform

- Integration of existing RISC-V ecosystem into a unified framework for design automation
- Specification-driven design process where user requirements inform system configuration
- Template-based approach with parameterization for rapid design exploration
- Automated consistency checking between different design views throughout integration
- KPI-driven generation process where users specify performance targets instead of manual configurations
- Iterative optimization approach that explores multiple design alternatives until objectives are met
- Customization workflow that enables interoperability with existing design environments
- Iterative exploration of multiple floor-planning options to find optimal solutions
- Hierarchy manipulation to enables rapid adaptation to change physical requirements



Typical Results from Test Point Exploration

- Multiple Man-Months of development time saved in RTL design
- Design time reduced from weeks to hours for complex SoCs
- Successfully achieved aggressive PPA (Performance, Power, Area) targets unreachable with manual methods
- Enabled faster exploration of multiple design alternatives
- Demonstrated die size reduction through optimized hierarchy reorganization
- Increased design and IP reusability in production environments
- Eliminated design inefficiencies such as long loops, loopbacks, and redundant ports

Conclusion

- Defacto's design solution helps RISC-V SoC designers manage increasing complexity
- Automation enables multiple iterations to find optimal design configurations
- Front-end integration process simplifies generation of different design configurations
- Customization possibilities increase interoperability with internal design environments
- Platform helps reach challenging and sometimes contradictory KPI objectives

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