RISC-V as an ASIP Platform for Portable Hearing Aid Devices

Sven Schönewald[1]*, Viktor Schneider[1], Simon Klein[1] and Holger Blume[1]

[1]Institute of Microelectronic Systems, *Leibniz University Hannover*, Hanover, Germany

Abstract

Hearing loss is one of the most prevalent sensory impairments. The use of hearing aids with adaptable personalized signal processing has the potential to further enhance the social lives of those affected. To develop and evaluate novel hearing aid algorithms, high-level programmable, low-power, and portable behind-the-ear (BTE) research platforms are required to conduct studies in real-world settings. However, the market for hearing aid processors is highly restrictive and often relies on proprietary and closed source signal processors. As a key component towards an open source hearing aid, this paper presents an overview of the performance of two different state-of-the-art hearing aid algorithms on a RISC-V based application-specific instruction set processor (ASIP). A number of standard instructions set extensions (ISEs) are profiled and synthesized for a 22nm technology. A systematic survey of the performance reveals a requirement for specialised, custom hardware. The processor is further optimised using a custom coordinate rotation digital computer (CORDIC) unit for non-linear calculations.

Introduction

It is estimated that approximately 430 million individuals currently experience disabling hearing loss. According to the World Health Organization (WHO), this number is expected to rise to 700 million by 2050 [1]. To address this issue, hearing aids are becoming increasingly compact, which presents challenges for accommodating the digital signal processor necessary to process increasingly complex algorithms.

Today, the market for hearing aids is dominated by five major manufacturers, who collectively hold 99% of the market share [2]. Access to their architectures is limited to selected research organizations [3]. Consequently, there are few available research platforms based on open source hardware.

To address these challenges, this extended abstract presents a design space exploration for the execution of two state-of-the-art hearing aid algorithms on the IBEX RISC-V processor [4]. Standard extensions, as well as one custom extension, are evaluated. To enable the evaluation, a front end synthesis is performed using a 22nm fully depleted silicon on insulator (FD-SOI) [5] technology commonly used for low power applications. In this way, the resulting area and energy metrics can be compared to the increased performance.

Algorithms

One key challenge in hearing aid software is the requirement for energy efficient computing. For this reason, algorithms are implemented using fixed-point arithmetic. To balance audio quality with execution time, a comprehensive analysis of the numeric range of the different variables has to be carried out. To achieve this, a MATLAB based framework was used to carry out both the initial fixed-point analysis, as well as the conversion to C code. Two algorithms were chosen for an evaluation. These are the monaural loudness compensation (MLC) [6], used to adjust the audio spectrum to match a patients hearing loss. And the minimum variance distortionless response (MVDR) beamformer [7] which can be used filter out noise and focus on speech. Both of these algorithms operate in the frequency domain. For this reason, the size of the FFT window and corresponding spectrum affects the execution speed. For this evaluation, a 256 point FFT is used, consisting of 64 new samples, 64 samples from the previous frame, and 128 zeros for padding to avoid aliasing. For simplicity, the constant FFT/iFFT overhead is excluded from the following evaluation. An initial analysis of the algorithms reveals that the MLC algorithms run time significantly exceeds the MVDR. The MLC is therefore analysed further, and a hotspot is identified in the calculation of logarithmic functions required for the compression step. To alleviate this, an initial optimisation is a software based implementation of the coordinate rotation digital computer (CORDIC) algorithm [8]. This is added to the MATLAB framework, enabling it to automatically generate code with matching fixed-point formats for these functions.

Hardware

As a basis for the evaluation of run time, area and power, the IBEX open source core was chosen. It

*Corresponding author: schoenewald@ims.uni-hannover.de

features a 32-bit data path suitable for embedded applications. Additionally, it can be modified using a number of design parameters to achieve optimal performance for a given application.

For this work, the two build-in configurations *small* and *maxperf* are considered.

Additionally, the IBEX was further extended by two methods

- A *optimised* configuration was created by modifying the parameters of the *maxperf* configuration, including the B-extension and a branch-predictor
- A *custom* configuration was created by adding a custom CORDIC hardware unit, to further optimize logarithmic calculations

This custom CORDIC hardware relies on a look-up table for the angles, as well as internal registers for the state. In this way, after an initial set of initialisation instructions, no more reads or writes to the general purpose register file are necessary. The state of the CORDIC is updated and read using dedicated step and read instructions. All instructions for this extension are situated in the *custom0* opcode field.

The custom CORDIC instructions are utilised through intrinsics in the C code. These are also fed back into the conversion process of the MATLAB framework, enabling it to automatically include them in logarithmic functions.

Evaluation

All configurations are initially evaluated in terms of their computational performance as shown in Figure 1. We observe a speedup of 34% from *small* to *optimised* for the MVDR and a similar value of 31% for the MLC. The MLC algorithm is further accelerated by 6% by introducing the CORDIC unit described in the previous section.

A clock frequency of 50MHz is chosen to achieve low power consumption. The audio is sampled at a rate of 16kHz typical for hearing aid applications [9]. Thus, a total of 200k cycles are available to process one frame of 64 samples. Either of the evaluated algorithms can be executed in real time under these constraints, with the MVDR taking 90k cycles and the MLC 141k cycles after all proposed optimisations are applied.

To compare the efficiency of the different implementations, the area, time and energy (ATE) product is calculated for the execution of the MLC algorithm and normalised to the baseline *small* configuration. The highest efficiency is achieved by the *maxperf* configuration with a reduction of 23%, whereas the fastest (*custom*) configuration is comparatively less efficient. This is due to the area requirements of the look-up table and state registers, which will be the subject of further optimisation.

Conclusion

This work demonstrates the viability of the RISC-V ISA as a baseline for digital signal processing of hearing aid algorithms. We achieve significant speedup by adjusting the selection of standard ISEs, as well as introducing a custom CORDIC extension for non-linear computation. This suggests that, with further optimisation of ISE selection and micro architecture, utilisation of the open source RISC-V standard in hearing aids will be an alternative to existing closed source or proprietary solutions.

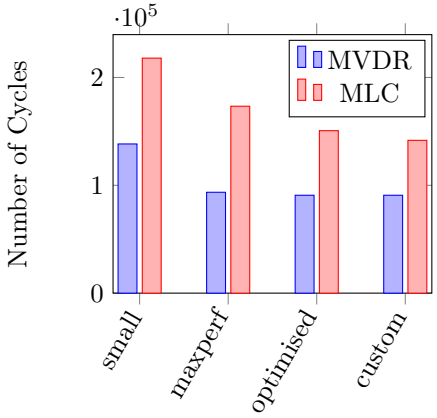

Figure 1: *Cycles for execution of MVDR and MLC*

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