Sovereignty – Independence – Innovation
7 years of HW/SW codesign with RISC-V at CEA

Thomas Dombek — thomas.dombek@cea.fr

Head of CEA's LIST/DSCIN
Digital Systems and Integrated Circuits division

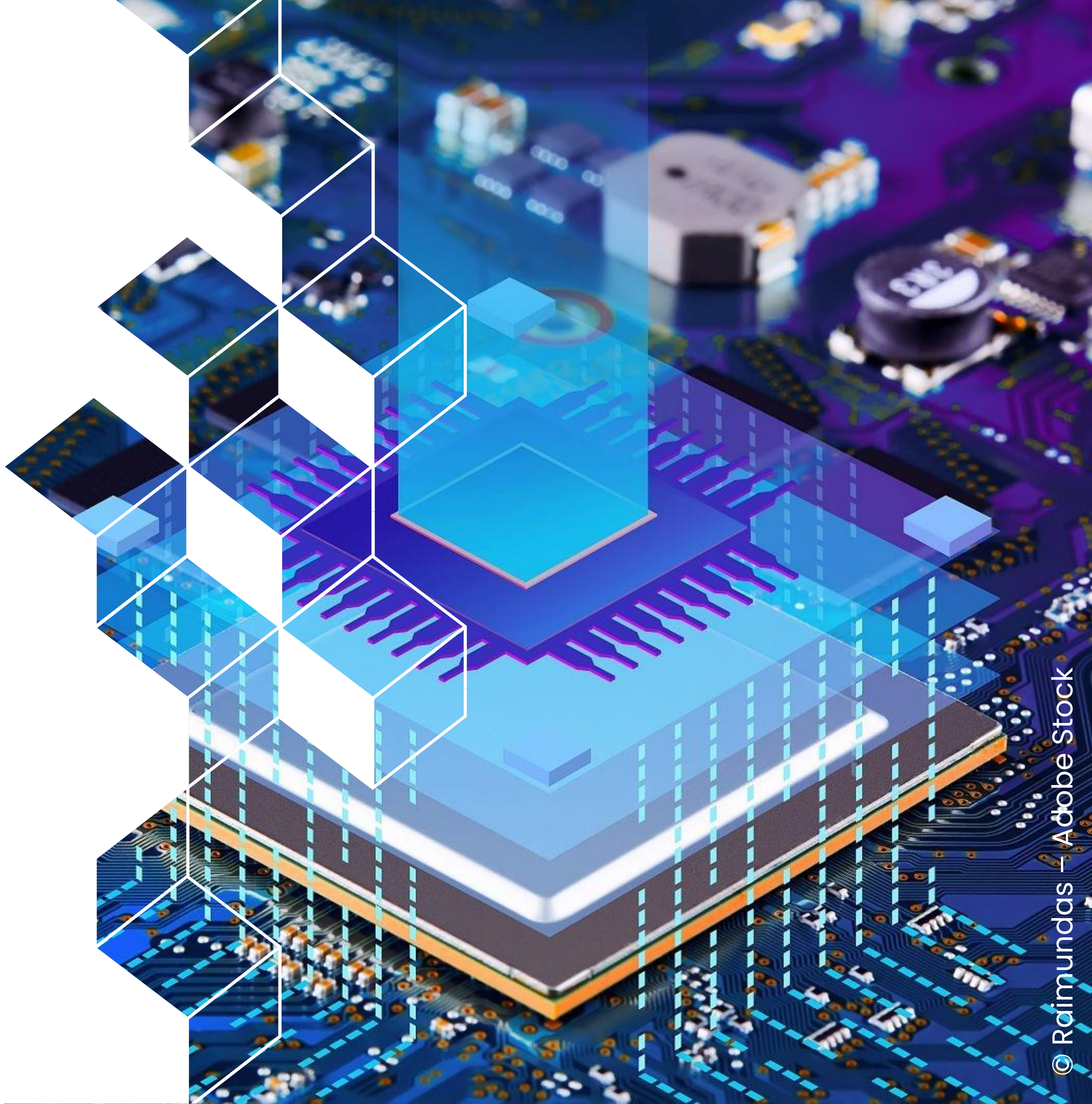
Thursday May 13th, 2025, RISC-V Summit Europe, Paris

Agenda

1. Design activities at CEA
2. RISC-V, the obvious choice
3. RISC-V related achievements
4. Perspectives

Design activities at CEA

From ultra-low-power (ULP) to high-performance computing (HPC)



CEA in a glimpse

21 000 employees

6 Billions€ of budget

700 industrial partners

650 patents/year

Most innovative organisations		TOP 100 GLOBAL INNOVATOR Clarivate Analytics
Government & academic research	**1st global**	2012, 2013, 2014, 2015, 2016, 2017, 2018, 2019, 2020, 2022, 2023, 2024, 2025

SECURITY DEFENSE

FUNDAMENTAL RESEARCH

LOW CARBON ENERGY

TECHNOLOGICAL RESEARCH

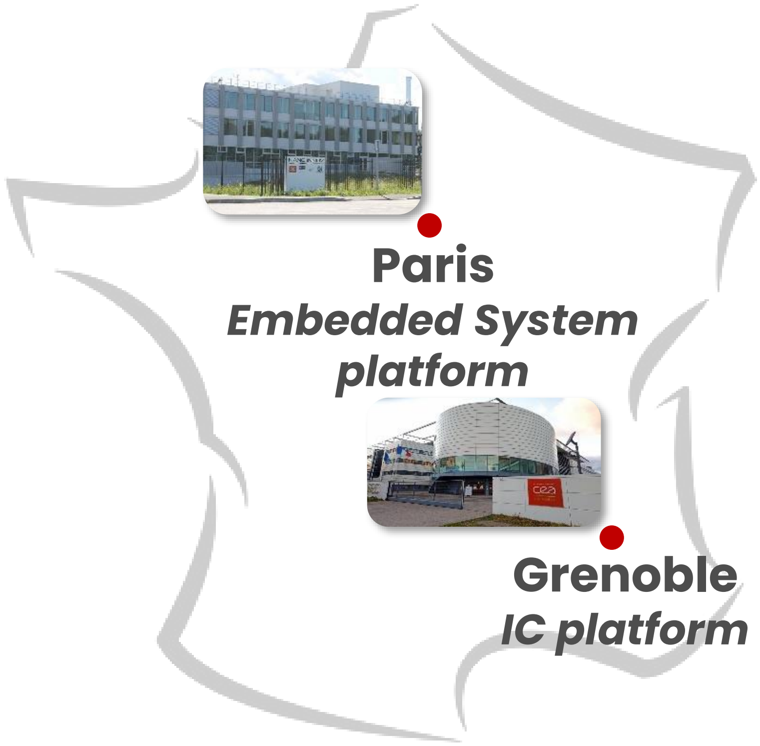
cea list

Smart digital systems

cea leti

Micro & nano-technologies

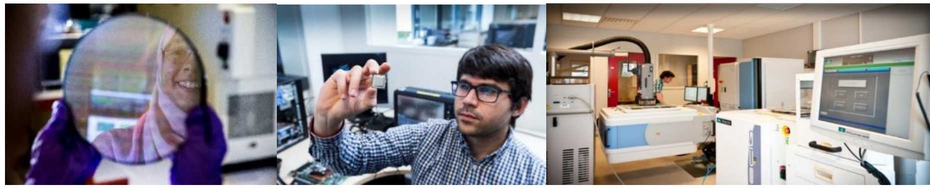
CEA in a glimpse



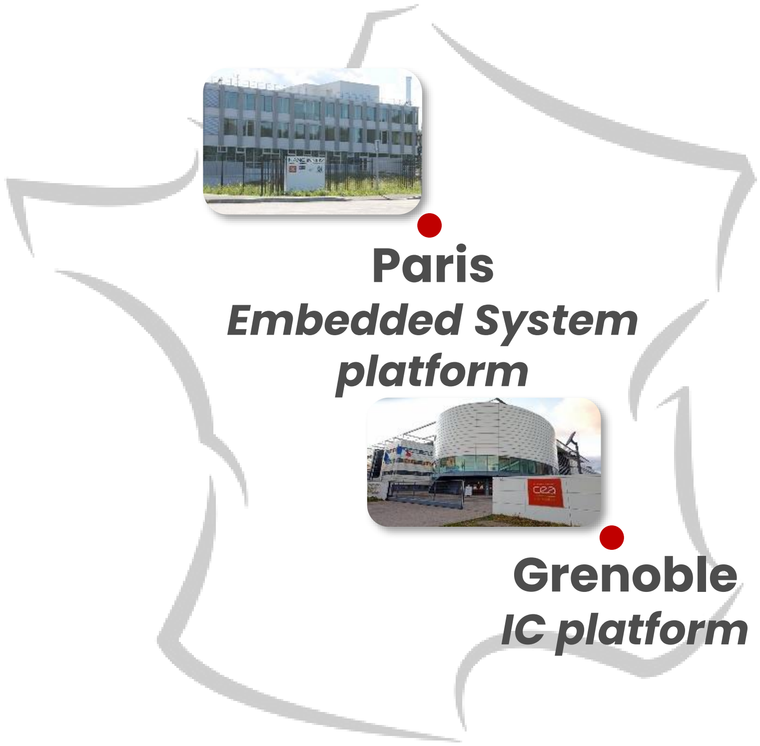
Smart digital systems

Micro & nano-technologies

- >2500 Staff members
- 11,700 sq. m of cleanroom space
  100-200-300 mm wafers
- >350 Industrial partners
- >600 Publications per year
- >3050 Patents in portfolio
- >75 startups created



CEA in a glimpse



cea list

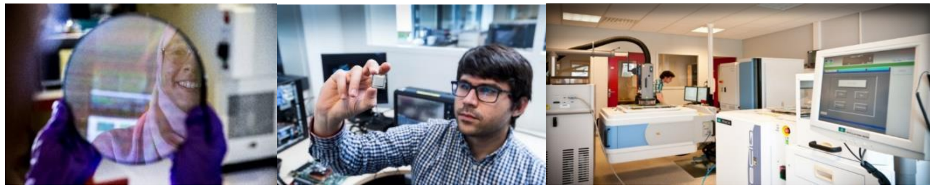
Smart digital systems

cea leti

Micro & nano-technologies

Lab-to-Fab Integrated Services from CEA:
https://www.youtube.com/watch?v=B6yqesaVMm4

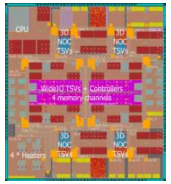
1. Expertise in designing state-of-the-art hardware architectures, systems-on-chip, ASICS, and chiplets.
2. Efficient development of reliable, secure, and low-power solutions tailored to your needs.
3. Utilization of advanced design exploration tools and state-of-the-art design flows to turn your idea into a ready-to-manufacture circuit.
4. Access to our cleanrooms for prototype manufacturing with extensive testing and verification at every stage of the design process.



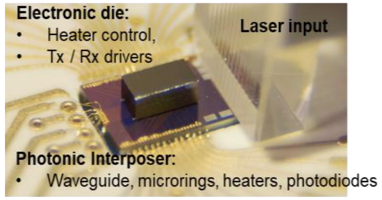
10+ years of experience in Chip design

Eco-innovation

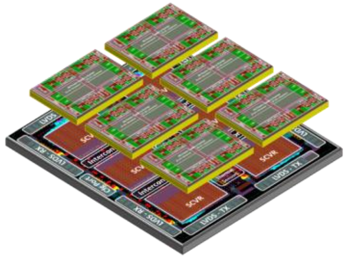
HIGH EFFICIENCY



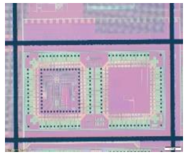
MAG-3D
3D Network-on-Chip



HUBEO
Photonic NoC interposer

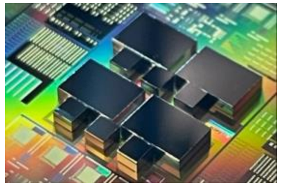


INTACT
6 chiplets & 96 processors



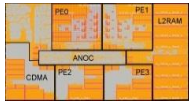
CRYOCMOS
Control for quantum computing

EPAC
HPC Variable Precision Accelerator

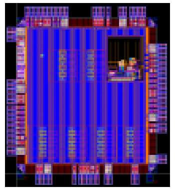


STARAC
Chiplet-based Optical Network on Chip

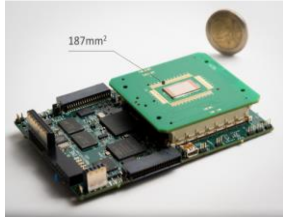
TRUST-WORTHY



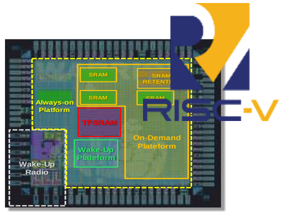
LOCOMOTIV
Adaptive Voltage & Frequency Scaling



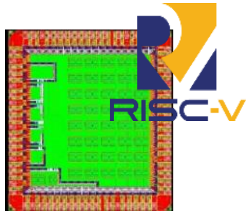
FRISBEE
ULP FDSOI



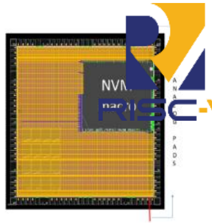
RETINE
Ultra-fast smart imager



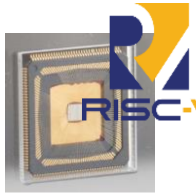
WARRIOR
RISC-V IoT IC with wake-up



Cyber-VT
Test Vehicle for IoT security enhancement

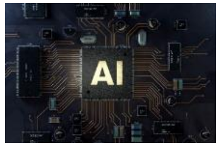


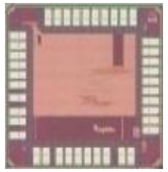
Non-Volatile-Memory
NVM subsystem for Microcontrolers



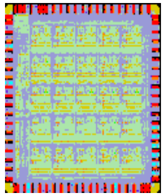
VASCO 2
ASIC vehicle for component security

AI

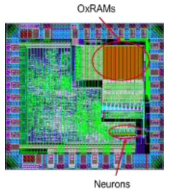




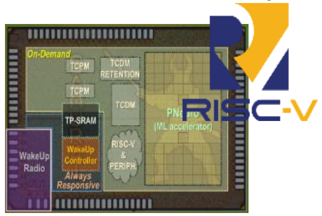
REPTILE
Analogue neuron



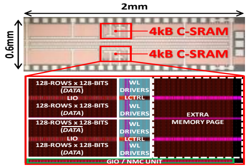
SPIDER
Neuromorphic DSP



SPIRIT
Spiking NN with eNVM

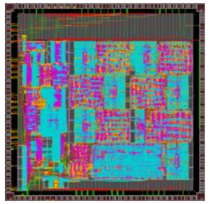


SAMURAI
IoT IC with NN accelerator



In-Memory-Computing
Compute-SRAM

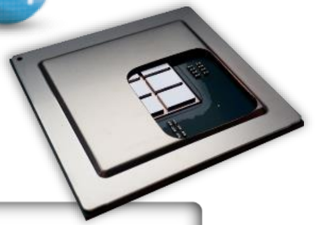
ESPERANTO
RNN with 50k synapses



NeuroCorgi
Ultra low power AI

2011 → 2024

INTACT - heterogeneity, modularity and reuse of 3D-Design



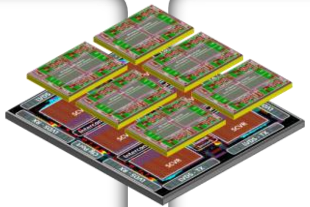
Making 3D design heterogeneity, modularity and reuse real

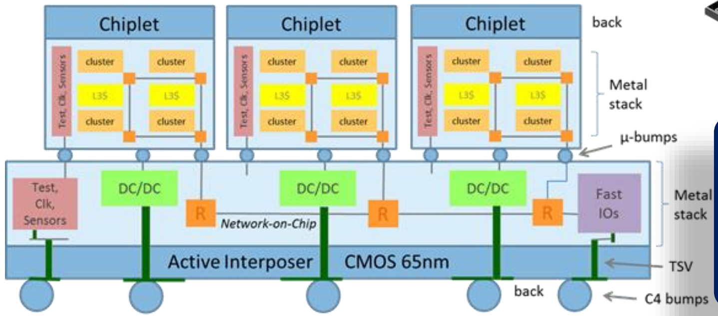
With further cost, TMM and yield improvements

Proven with our 96-cores compute demonstrator:

6 chiplets stacked on an active interposer

System Architecture





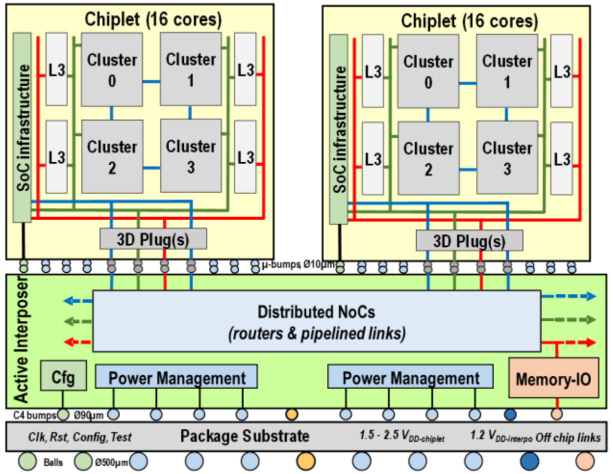
JSSCC'2020
Symposium'2016
3DIC'2015
ISVLSI'2015

3D-System architecture, smart chiplet design and IPs with key performance assets:

- **Scalability:** Cache-Coherency IP up to 512 cores with 3 levels of caches
- **High throughput @ ultra low power inter-layer connectivity:** ***(3Tb/s/mm2; 0,59pJ/bit)*** **:** 3D-Plugs inter-layer communication IP
- **Energy efficiency *(up to 81%)*:** Power management integrated in interposer
- **Ultra Low Latency *(0.6ns/mm)*:** Asynchronous NoC IP

Enable heterogeneity, modularity and reuse of 3D-Design

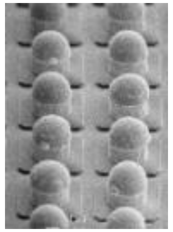
Design



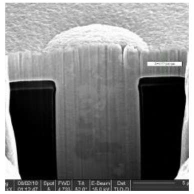
Heterogeneous 3D partitioning with:

- 28nm FDSOI chiplets (x6)
  - Low power compute fabric
  - Wide voltage range (0.5V – 1.3V)
  - Body biasing for logic boost & leakage ctrl
- 65nm active interposer
  - Power unit (Switched Cap DC-DC conv.)
  - Interconnect (Network-on-Chip)
  - Test, clocking, thermal sensors, etc

Technology



µ-bumps
Ø 10 µm
Pitch 20 µm



TSV
Ø 10µm
Height 100µm

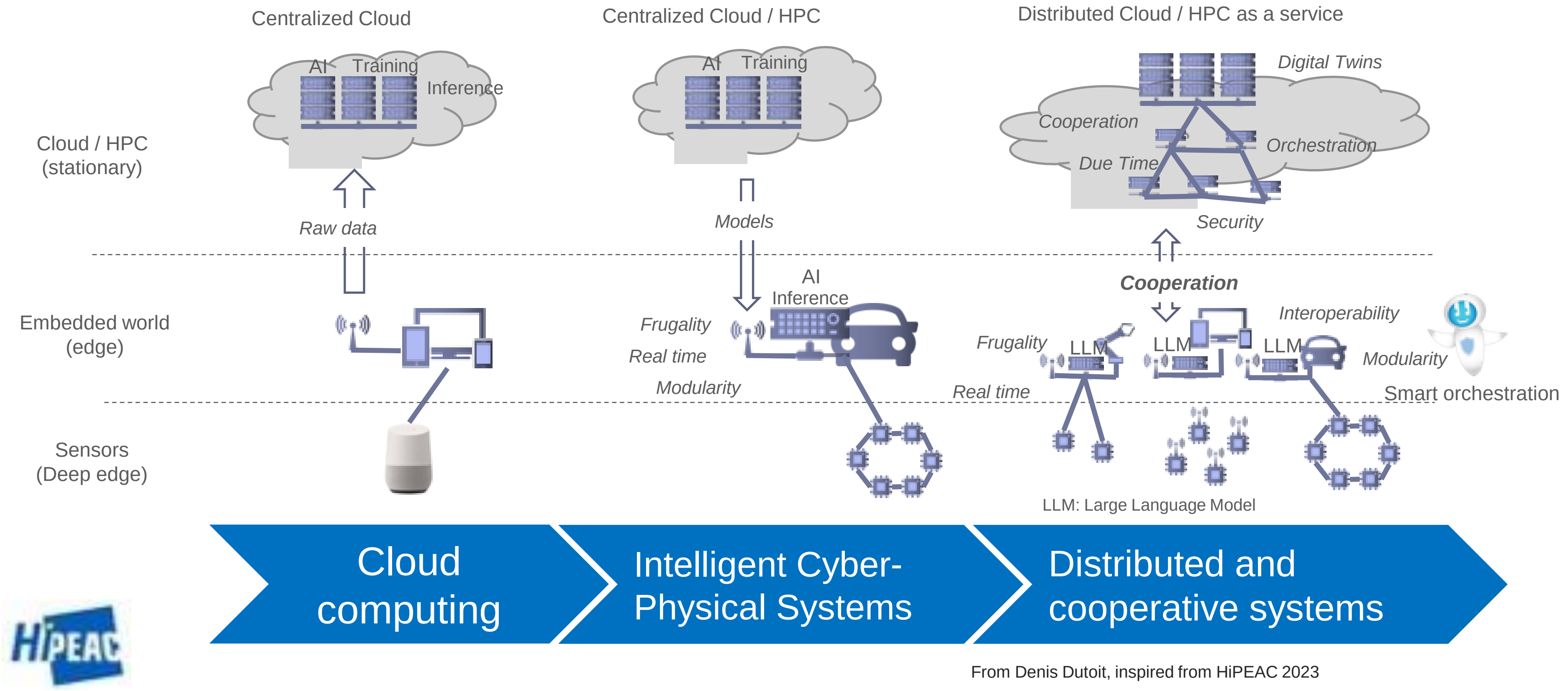
RISC-V, the obvious choice

Open-HW as a key to succes

Enhancing technology access to the real world. Source: Generated via Dall-E.

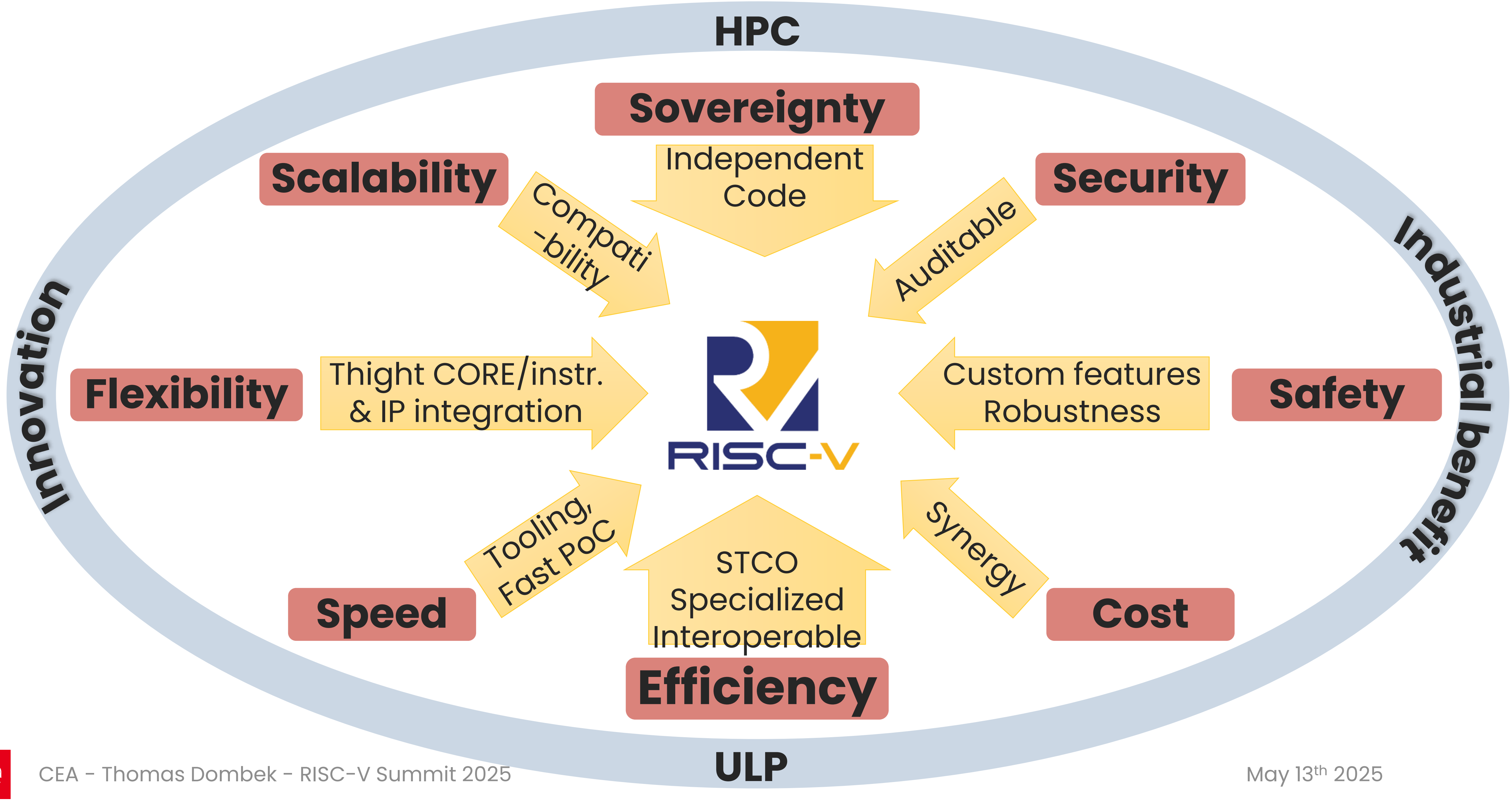
Towards the Next Computing Paradigm

(Aligned with the European HiPEAC roadmap vision)

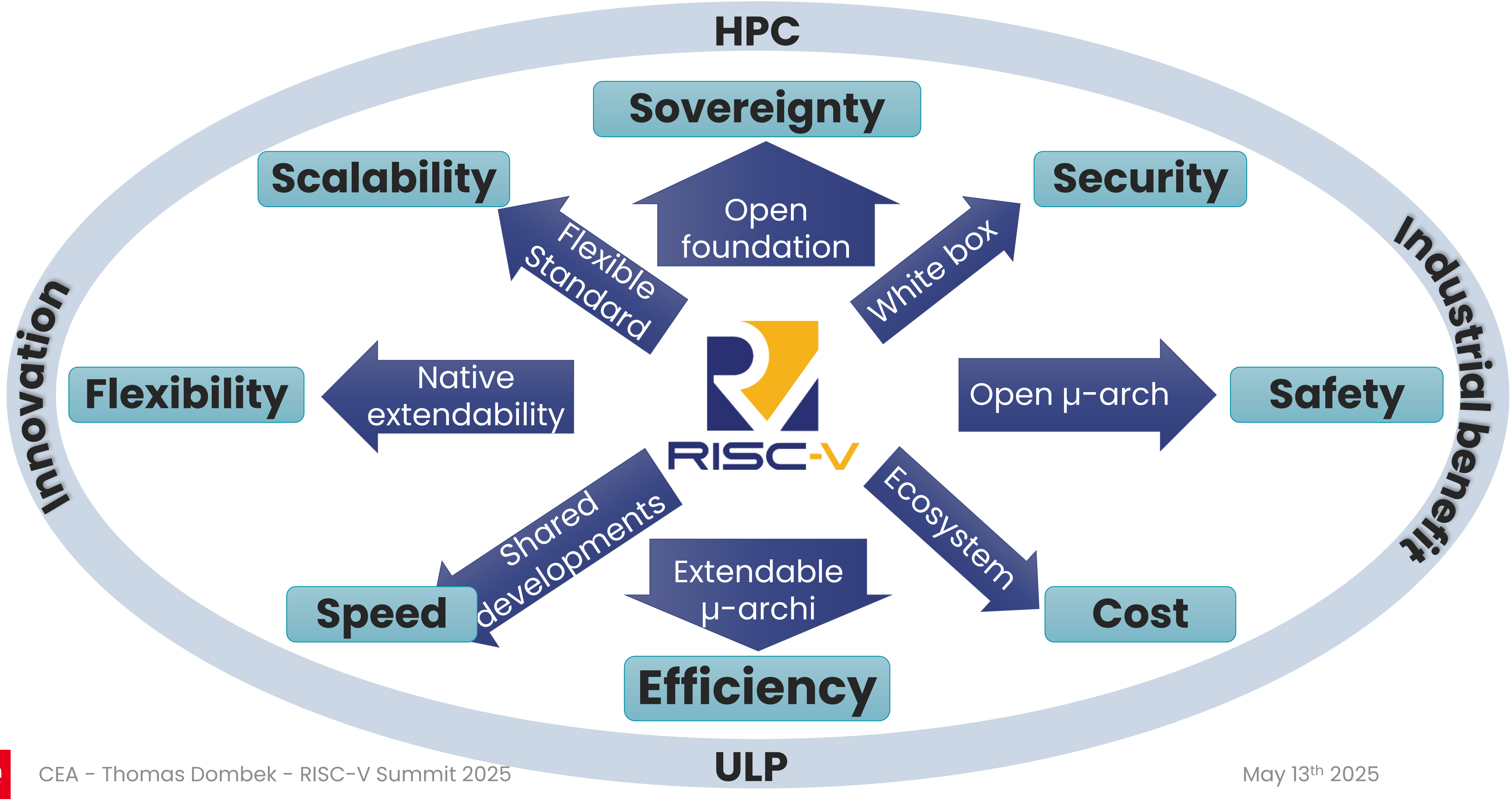


From Denis Dutoit, inspired from HiPEAC 2023

Design Space Challenges



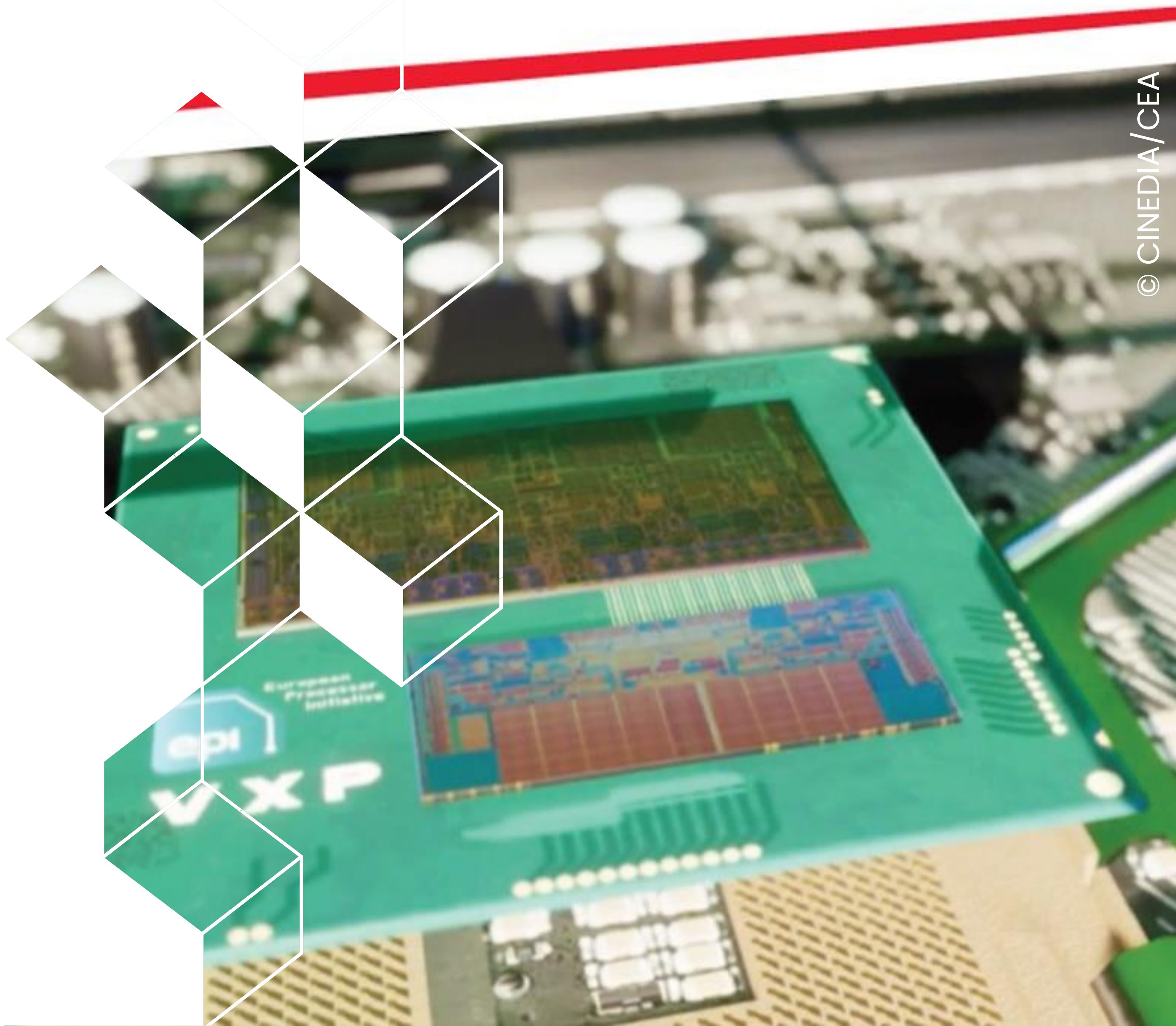
RISC-V & Open HW approach



RISC-V related achievements

From ULP to HPC

RISC-V OPENHW GROUP ECLIPSE FOUNDATION



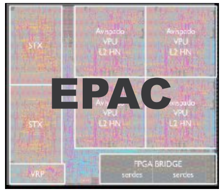
CEA RISC-V projects on a wide spectrum

HPC

Innovation

Industrial benefit

Sovereignty

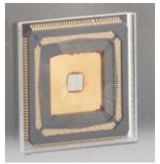


HPC Variable
Precision Accelerator

Scalability

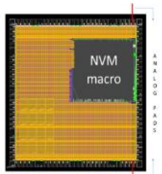
HPDcache:
High-Performance
L1 Data Cache

Security



VASCO
ASIC vehicle for
component
security

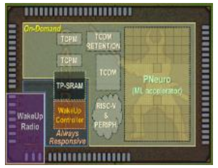
Flexibility



Non-Volatile-Memory subsystem
for Microcontrolers

Safety

Speed



SAMURAI IoT IC
with NN accelerator

Efficiency

Contributions to cores: CV32E40P, CVA6
Core building blocks
- GPIO, UART, SPI, Interrupt controller
- Low latency OBI interconnect

Cost

Suite of verification utilities
- UVM agents (AXI, SPI)
- Models of memory, flow control, clock & reset, watchdog
- Performance monitors

ULP

High-Performance L1 Data Cache for RISC-V Cores (HPDcache): high throughput, flexible solution

3x Bandwidth increase
Becoming the standard CVA6 cache: used in future products

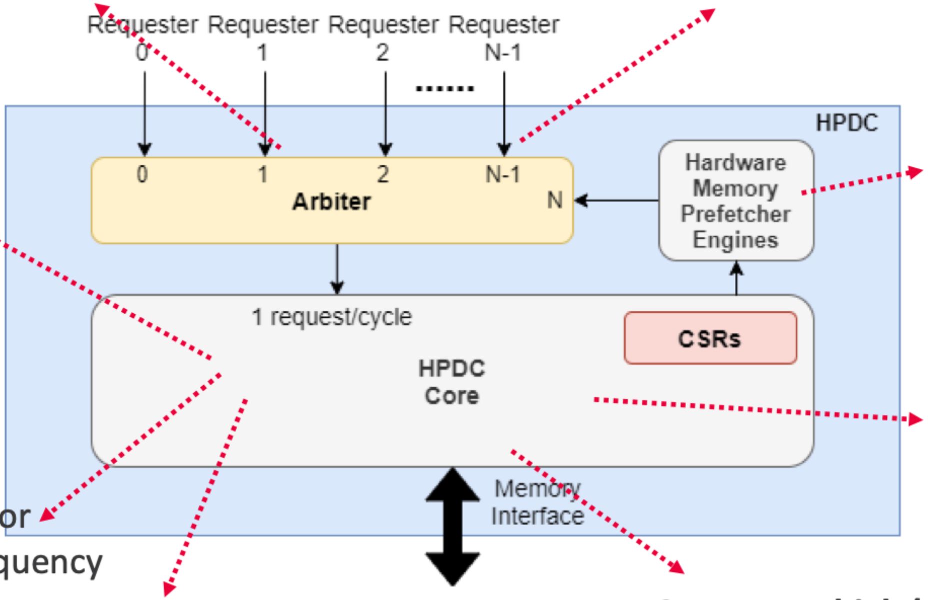
Industrial-grade verification
with UVM testbench (also open-sourced)

https://github.com/openhwgroup/cv-hpdcache
and
https://github.com/openhwgroup/cv-hpdcache-verif

Ref.: César Fuguet. HPDcache: Open-Source High-Performance L1 Data Cache for RISC-V Cores. *In Proc. of the 20th International Conference on Computing Frontiers (CF '23). DOI: 10.1145/3587135.3591413*

Support of multiple independent requesters:
CORE-V core, tightly-coupled accelerators

Allow high and flexible bandwidth
between the cache and the « requesters ».



Set-associative cache with configurable number of sets and ways.

Support of standard load, store, CMOs and atomic operations of the RISC-V ISA

Pipelined micro-architecture for high-throughput and clock frequency

Programmable hardware memory prefetcher with multiple engines for strided memory accesses.

Write-through cache:
Implements a write buffer supporting write coalescing and multiple inflight requests
(we plan to support write-back).

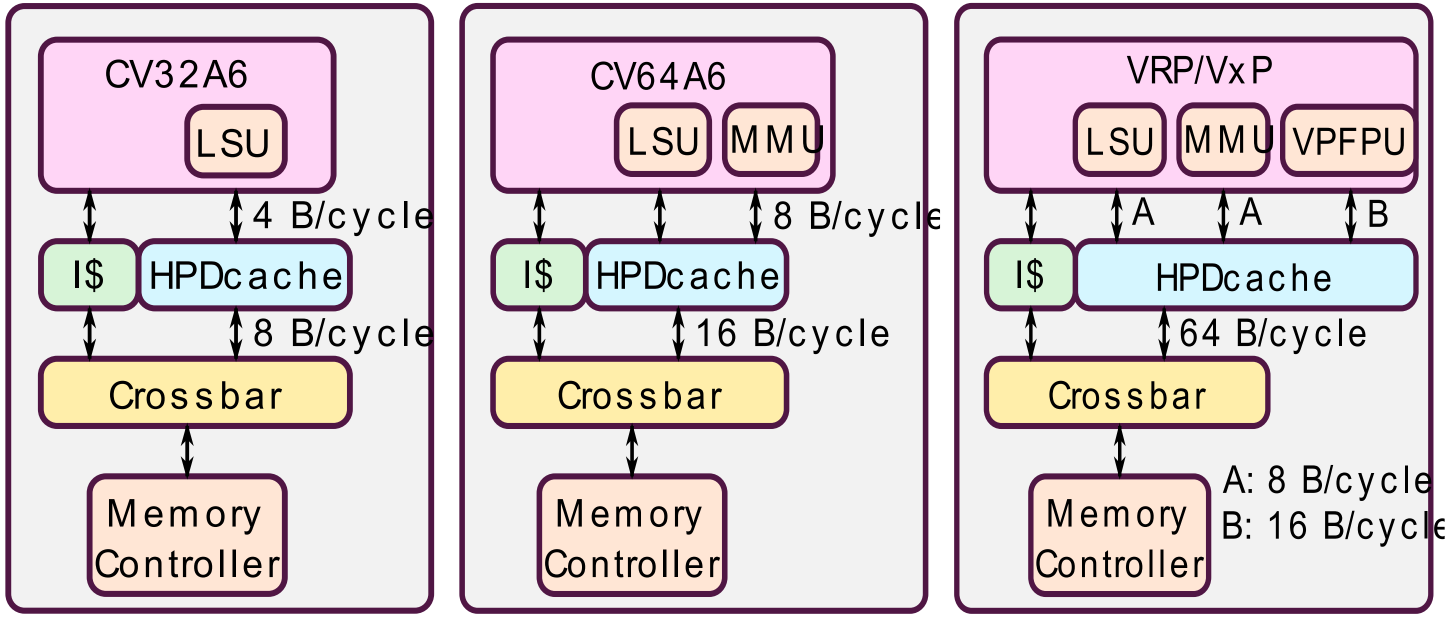
Supports a high (configurable) number of miss requests to the memory.

Allow out-of-order execution of memory operations to avoid unnecessary stalls (with compliance with the RISCV RVWMO consistency model).

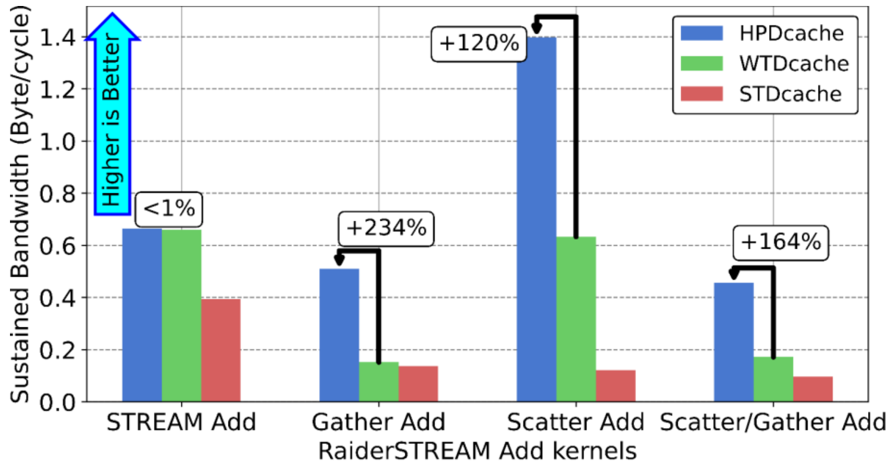
Adapter for the AMBA AXI5 interface on the NoC/memory side

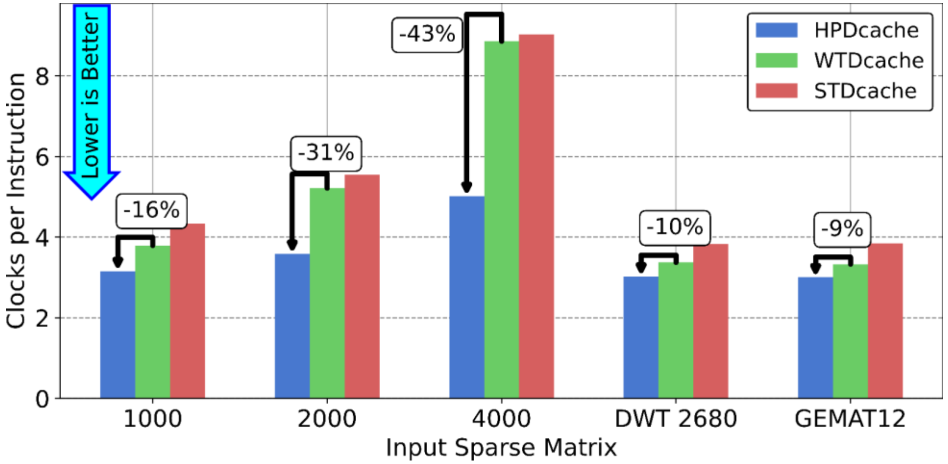
Successful Integrations in CVA6

Embedded (32 bits) Configuration | **Application (64 bits) Configuration** | **VRP/VXP [3] Accelerator Configuration**



Results obtained with RAM fixed access latency of 100 clock cycles on the ***application configuration*** [2]





VRP/VXP = CVA6 RISC-V core with ISA extension :

- Additional register bank
- New L1 D/I caches (incl. prefetchers) and LSUs
- Additional functional unit and instructions

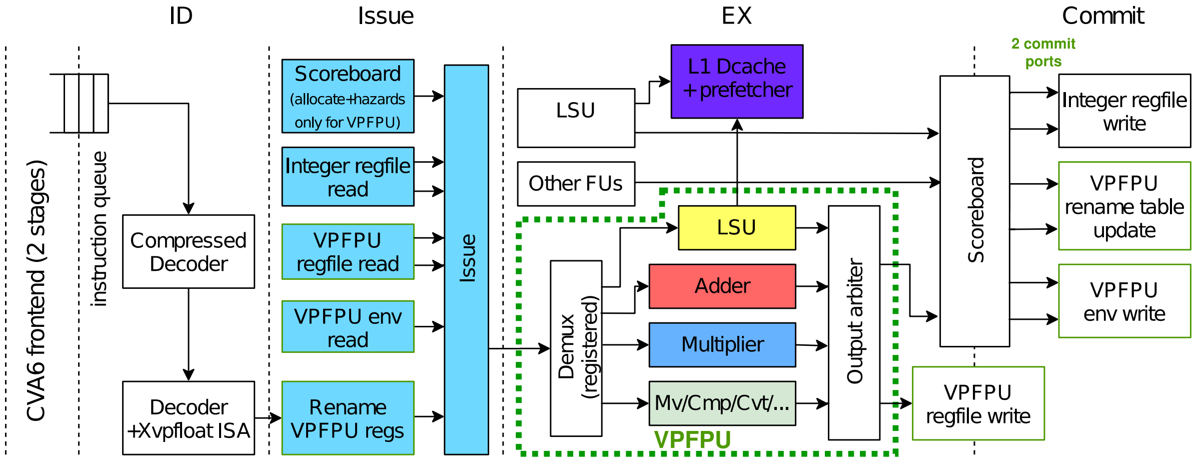
Negligible area overhead: +5.92% compared to CVA6-WTDcache

VRP/VXP: RISC-V Accelerator for Variable eXtended precision computing

Motivation: Software emulation (e.g. MPFR) too slow

Goal: be application-agnostic and limited by memory bandwidth instead of arithmetic

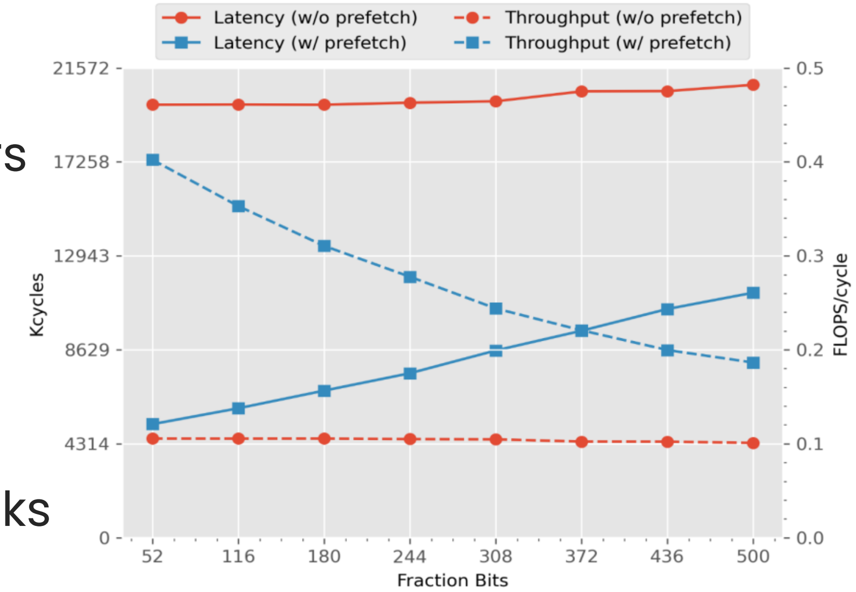
⇒ Variable extended Precision Floating Point Unit (VPFPU) integration in modified RISC-V CVA6 processor



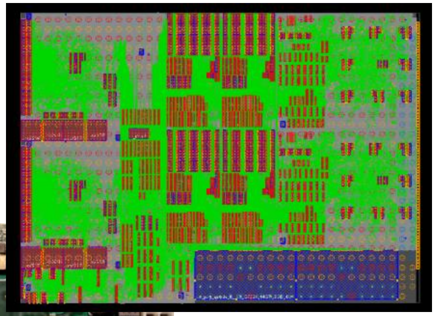
Main CVA6 modifications:

- 32 logical/64 physical 540-bit registers
- Register renaming
- OoO execution
- Linked to HPDcache
- 7 VPFPU functional units
  - Working iteratively on 64/128b chunks

⇒ Performance depends on precision



The coalescing write-buffer and multi-entry MSHR (**up to 128 outstanding read misses**) together with a hardware prefetcher provides a 5x throughput improvement



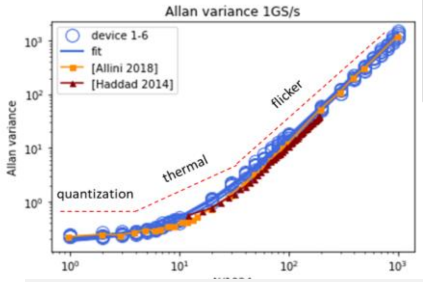
European Processor Initiative

epi

TRISTAN'24 (Graz, Austria)
Sept. 11th 2024

VASCO Test Vehicle for Secure IPs

CORE security features and critical IP validated on silicon:



L. Benea and *al.*, ***On the Characterization of Jitter in Ring Oscillators using Allan variance for True Random Number Generator Applications***, DSD 2022

Secure processor with 3 protections

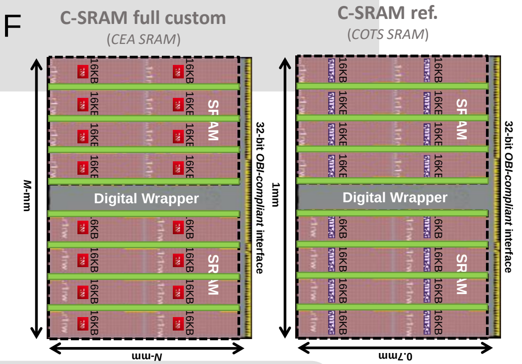
- Pipeline (CV32b demo on ASIC FD-SOI)
- Cache (FPGA 64b demo)
- Memory encryption (FPGA 64b demo)

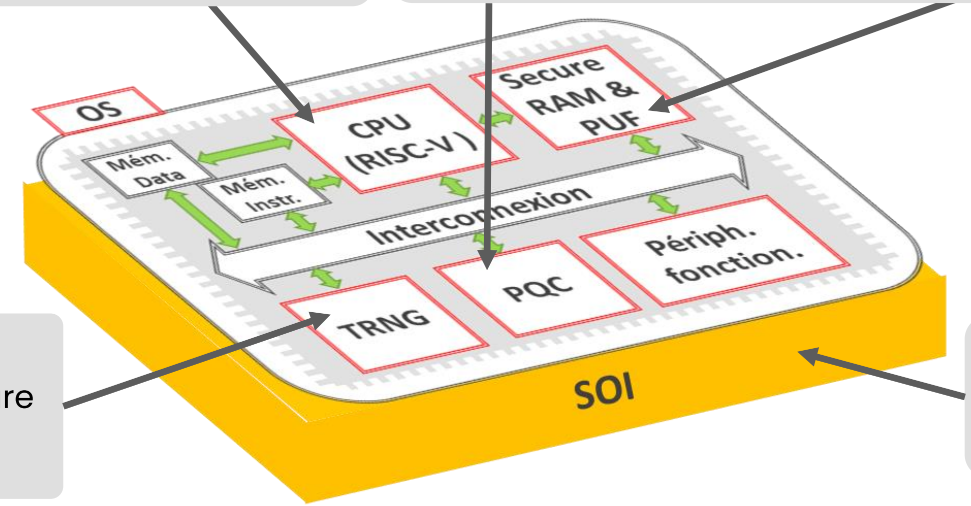
Advanced Cryptography

- Optimized and secure post-quantum cryptography (PQC) implementations
- FD-SOI oriented secure crypto-accelerator

Near memory computing

- C-SRAM for secure and crypto applications
- Secure SRAM: fast and frugal erase function
- SRAM-PUF

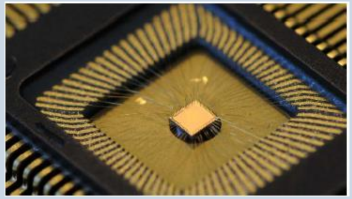




Innovative TRNG

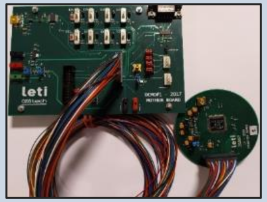
- FD-SOI oriented TRNG architecture
- Entropy sources modeling and characterization

FD-SOI oriented design for primitives and countermeasures



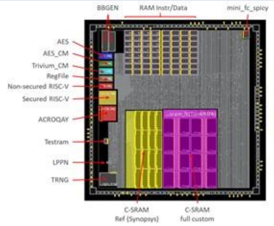
Bulk 28nm

VASCO#0: 2018



22FDX

VASCO#1: 2020



22FDX

VASCO#2: 2022

Updates on:
Secure Processor
IA Accelerator
PQC Accelator
RNG

22FDX

VASCO#3: Q4 2024

To define with our partners

VASCO#3.1: 2026

Designing & characterizing innovative cyber-security IP on ASIC

VASCO: ONE STOP SHOP FOR DESIGNING & CHARACTERIZING INNOVATIVE CYBER-SECURITY IP ON ASIC

Architecture

Feasibility analysis
Specifications
Enhancement
Benchmarking

Design

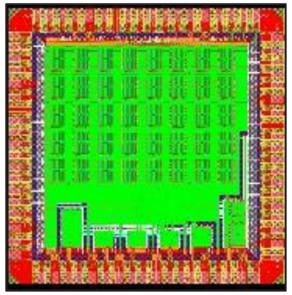
Specific IP Development & Integration
(Crypto-accelerator, TRNG, PUF…)

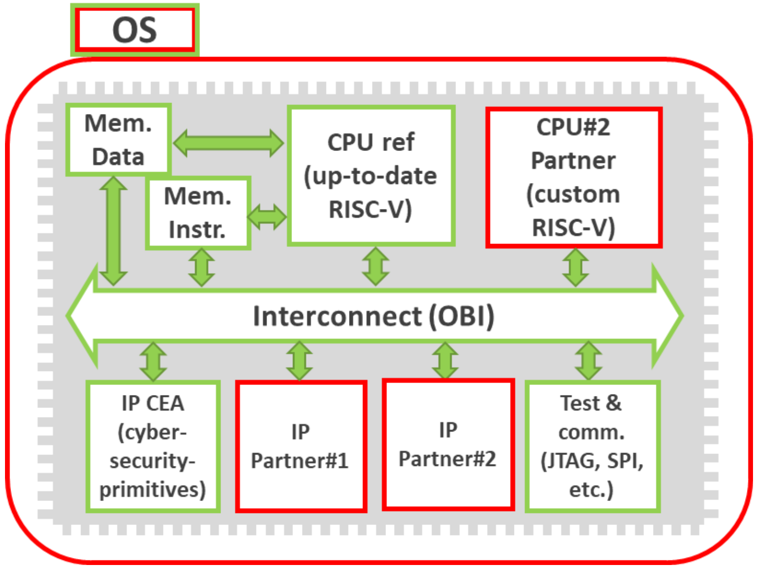
Prototyping

MPW Shuttle
Assembly & Test

Characterization

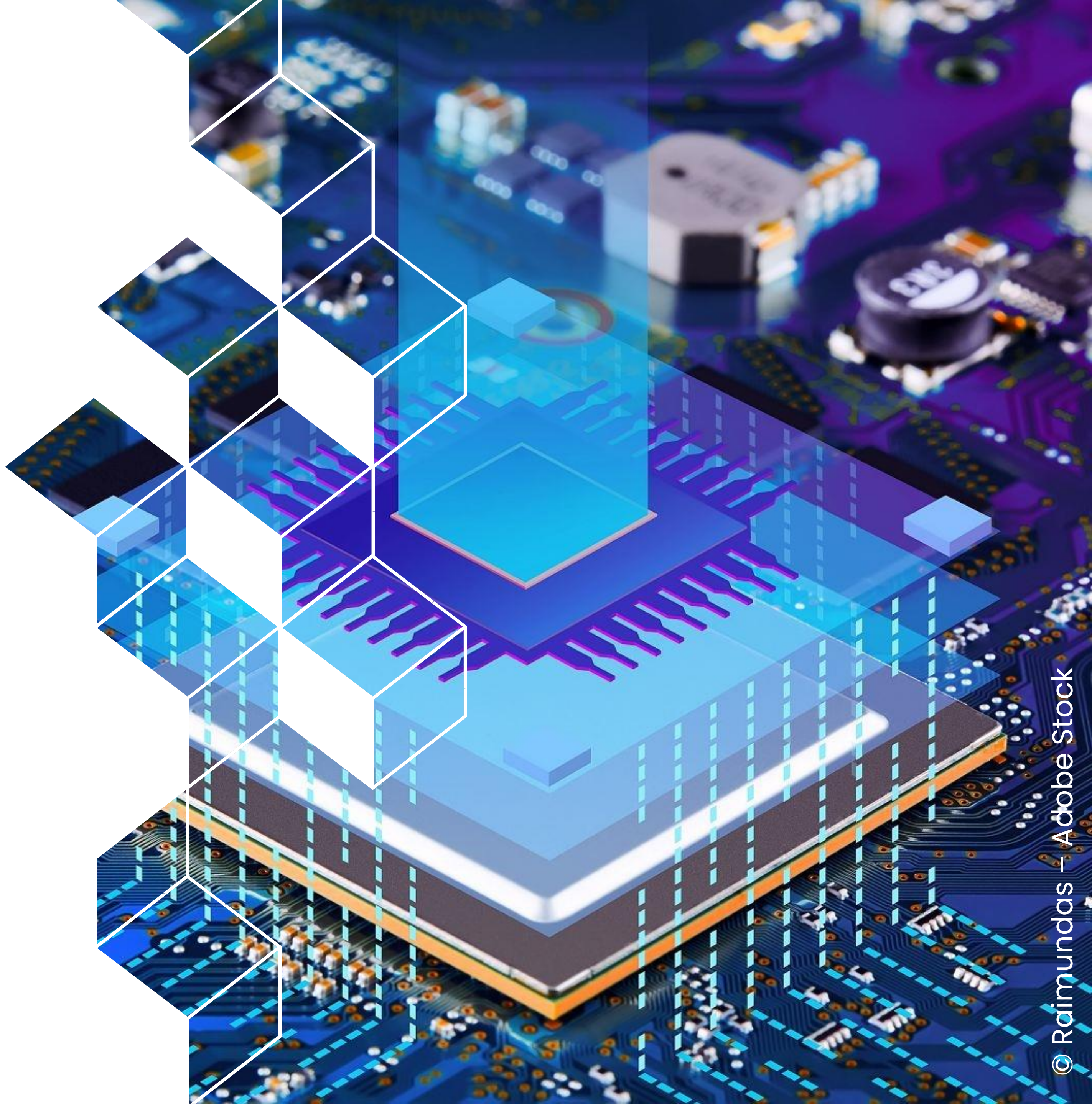
Hardware security tests
Performance tests





Perspectives

Collaboration and innovation



© Raimundas – Adobe Stock

Computing innovation through open collaborations

CEA is committed to support fast innovation and a sovereign open european ecosystem

RISC-V

Community Member

ISA Specification

OPENHW GROUP – PROVEN PROCESSOR IP

Platinium Member
Member of the Board of Directors

μ-processor design

ECLIPSE FOUNDATION

Strategic Member

Software and tools

Chips JU

TRISTAN RISC-V

- Fast and Efficient ML-based Power Modeling of Integrated Circuits
- Formal models combination for safety properties verification

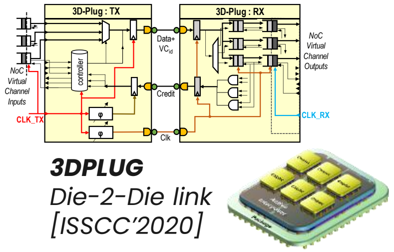
RIGOLETTO

- Modeling of extra-functional properties of Automotive High Performance RISCV core

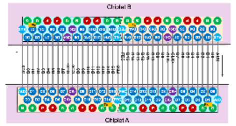
Perspectives

High Efficiency, Secure OpenSource Systems : Core + Memory + Interconnect
From 32- & 64- to future 128-bit architectures

Chiplet & System Interconnect

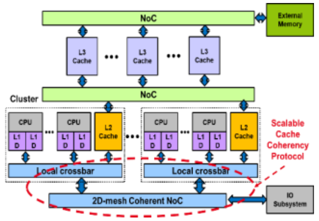


3DPLUG
Die-2-Die link
[ISSCC'2020]

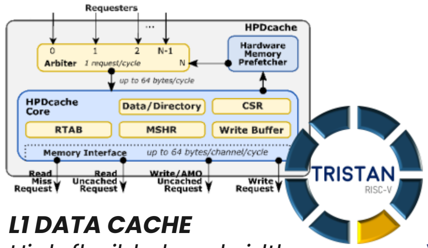


UCIe, ODSA
Die-2-Die link
for chiplet communication

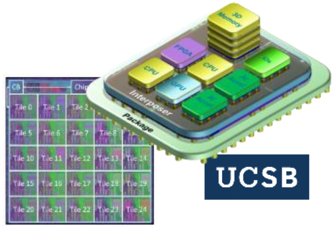
Memory Hierarchy & Caches



INTACT – FD28+65
MIPS 32-bit OpenSource Core
TSAR L1/L2/L3 Memory
Architecture



L1 DATA CACHE
High flexible bandwidth
Multiple Independent requesters
Out-of-order execution

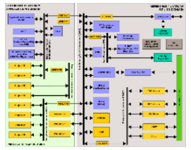


Open PITON
Sclalable Memory &
Interconnect hierarchy,
3D Chiplet partitionning

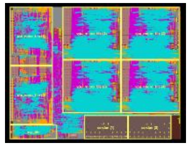
Towards a generic OpenSource Computing platform for heterogeneous architectures

HPC and new compute models targeting NCP

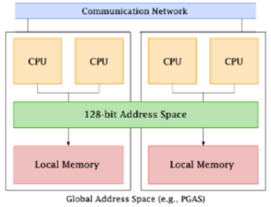
Computing Cores



PULP-based 32-bit
Low Power Efficient Platform
Used extensively for all
IoT & cybersecurity circuit



ARIANE-CVA6 64-bit,
GF22FDX
Host CPU for HPC
*(**<u>including VXP accelerator</u>**)*



RISC-V 128 bit
Global Address Space (GAS)
to reach thousands of nodes
+ Simulation, Compiler, etc
ANR MAPLURINUM

Safe and secure systems
Silicon evaluation & reference plateform

2018 2020 2023 2026 2030

Thanks for your attention!
Any question?

CEA at the RISC-V Summit Europe 2025

Booth #32

On display at our booth:
VXP & VASCO 2

Talks:

- "**Sovereignty, independence, innovation: 7 years of HW/SW codesign with RISC-V at CEA**" by Thomas Dombek (CEA). Keynote on Tue 13 at 10:00, in Gaston Berger (S2).
- "**VASCO: ASIC Test Platform for Cybersecurity on FD-SOI**" by Stefano Di Matteo (CEA). Demo pres on Tue 13 at 15:35, in Louis Armand East (S3).
- "**RISC-V based GPGPU on FPGA: A Competitive Approach for Scientific Computing?**" by Éric Guthmuller (CEA). Talk on Tue 13 at 17:00, in Gaston Berger (S2).

Posters:

- "**Implementing out-of-order issue in CVA6 for efficient support of long variable latency instructions**" by Eric Guthmuller (CEA). Poster on Tue 13, at island 2.1 on S2.
- "**CIAMH: Confidentiality, Integrity, and Authentication across the Memory Hierarchy**" by Karim Ait Lahssaine (CEA). Poster on Wed 14, at island 1.1 on S1.
- "**Pre-silicon Security Analysis of RISC-V Processors against Fault Injection Attacks**" by Damien Couroussé (CEA). Poster on Wed 14, at island 1.3 on S1.
- "**Comprehensive Lockstep Verification for NaxRiscv SoC Integrating RISC-V DV, RVLS, and Questa/UVM**" by Billal Ighilahriz (CEA), Poster on Wed 14, at island 2.1 on S2.
- "**RISC-V based GPGPU on FPGA: A Competitive Approach for Scientific Computing?**" by Éric Guthmuller (CEA). Poster on Wed 14, at island 3.1 on S3.
- "**RISC-V-based Acceleration Strategies for Post-Quantum Cryptography**" by Stefano Di Matteo (CEA). Poster on Wed 14, at island 3.1 on S3.
- "**TYRCA: A RISC-V Tightly-Coupled Accelerator for Code-Based Cryptography**" by Stefano Di Matteo (CEA). Poster on Wed 14, at island 3.1 on S3.
- "**Towards Efficient Modeling and Validation of Scalable Chiplet-Based Platforms**" by Fatma Jebali, Ayoub Mouhagir (CEA). Poster on Thu 15, at island 2.3 on S2.

Thomas DOMBEK

thomas.dombek@cea.fr