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RISC-V Real-Time Interrupt Architecture

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RISC-V Real-Time Interrupt Architecture

- Motivation
- Trap Stack Pointer Management
- Nested Vectored Interrupts
- Real-Time Interrupt Delivery
- Bus-less Single Core Configuration
- Latency and Area Impact
- RTIA Development Status

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RISC-V Real-Time Interrupt Architecture

Motivation

Requirement	RISC-V AIA
Real-Time (deterministic low latency) interrupts	❑ No
Multi-core configurations support	✓ Yes
Virtualization support	✓ Yes
Inter-processor interrupts	✓ Yes
RISC-V ISA compliance, incl. H-extension	✓ Yes
Unified programming model	✓ Yes
Flexible interrupt routing	✓ Yes
Bus-less single core	❑ No

Most features are covered by RISC-V Advanced Interrupt Architecture (AIA) which can be extended with:

- Nested vectored interrupts
- Low latency interrupt delivery
- Light weight real-time interrupt architecture

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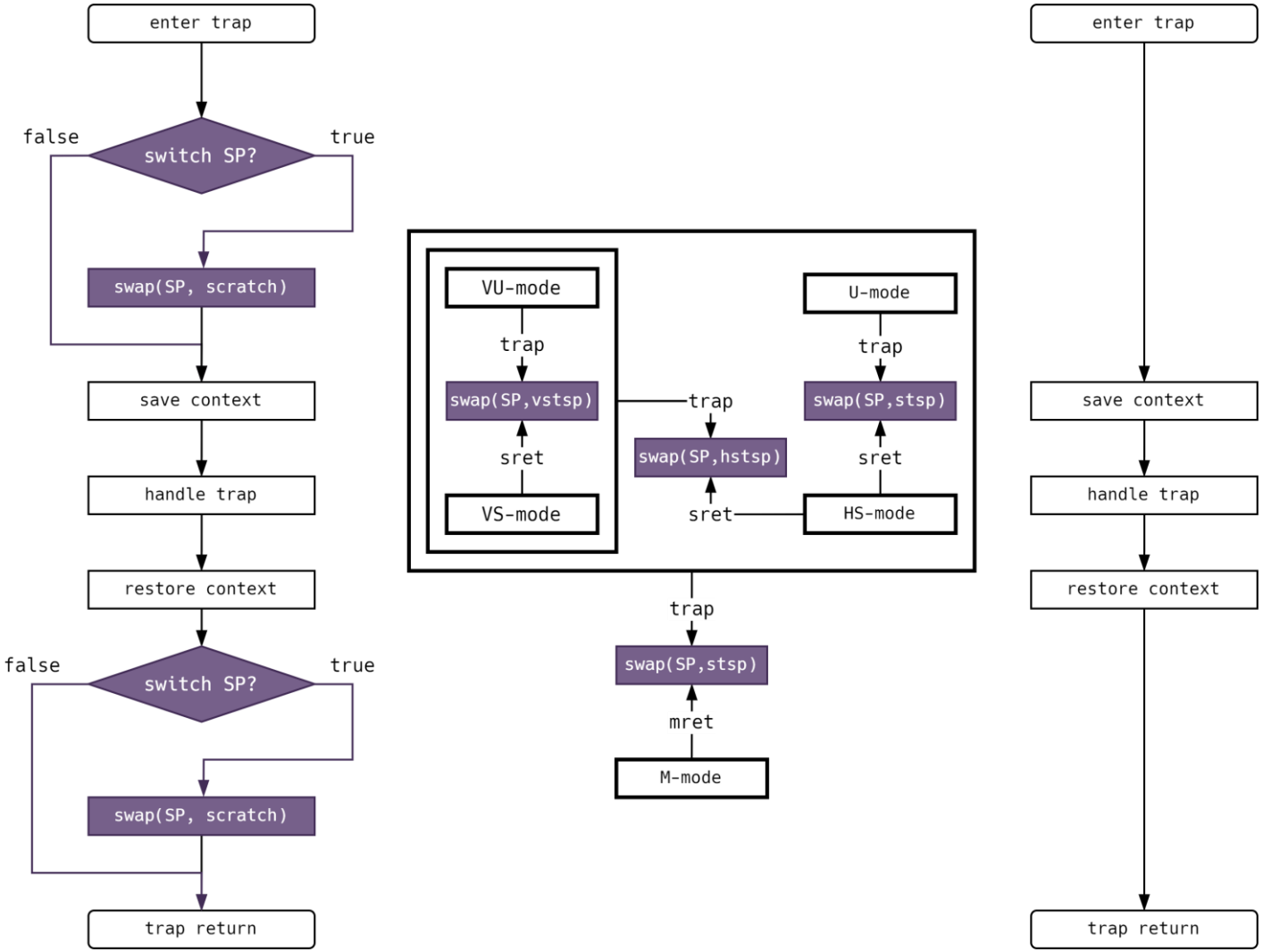
RISC-V Real-Time Interrupt Architecture

Trap Stack Pointer Management



- Avoid stack-less execution in trap handler
- Reduce context store/restore overhead
- Allow hardware to automate trap frame
- Run-time configurable for each privilege mode
- Compatible with all interrupt handling modes (Direct, Vectored)

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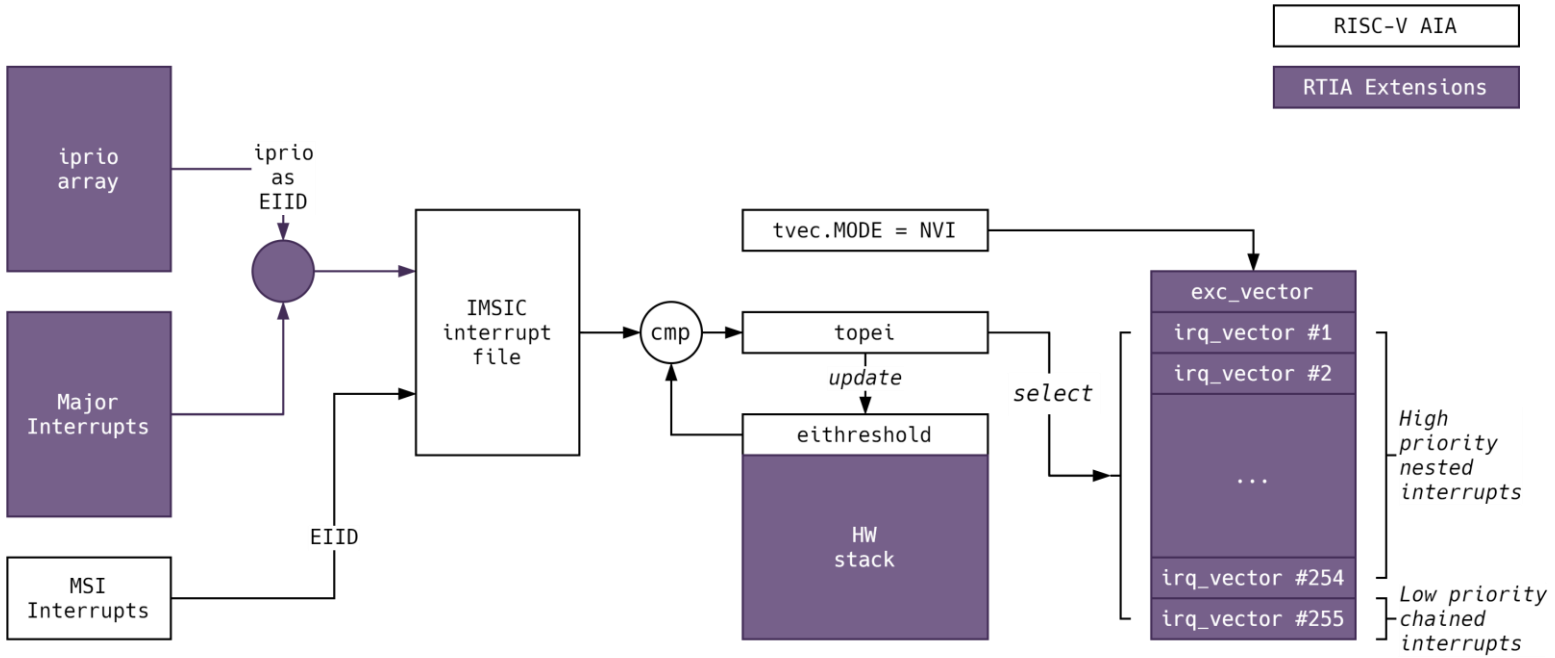
Nested Vectored Interrupts



- New *Nested Vectored* interrupt handling mode
- Major interrupt reporting via IMSIC file (use *iprio* as EIID)
- External interrupt vectors table:
  - Shared exception trap vector
  - Up to 255 high priority nested interrupts
  - Lower priority chained interrupt (share single vector)
- Automatic external interrupt claim and jump by vector
- Interrupt complete triggered from software
- Interrupt threshold update at interrupt claim/complete

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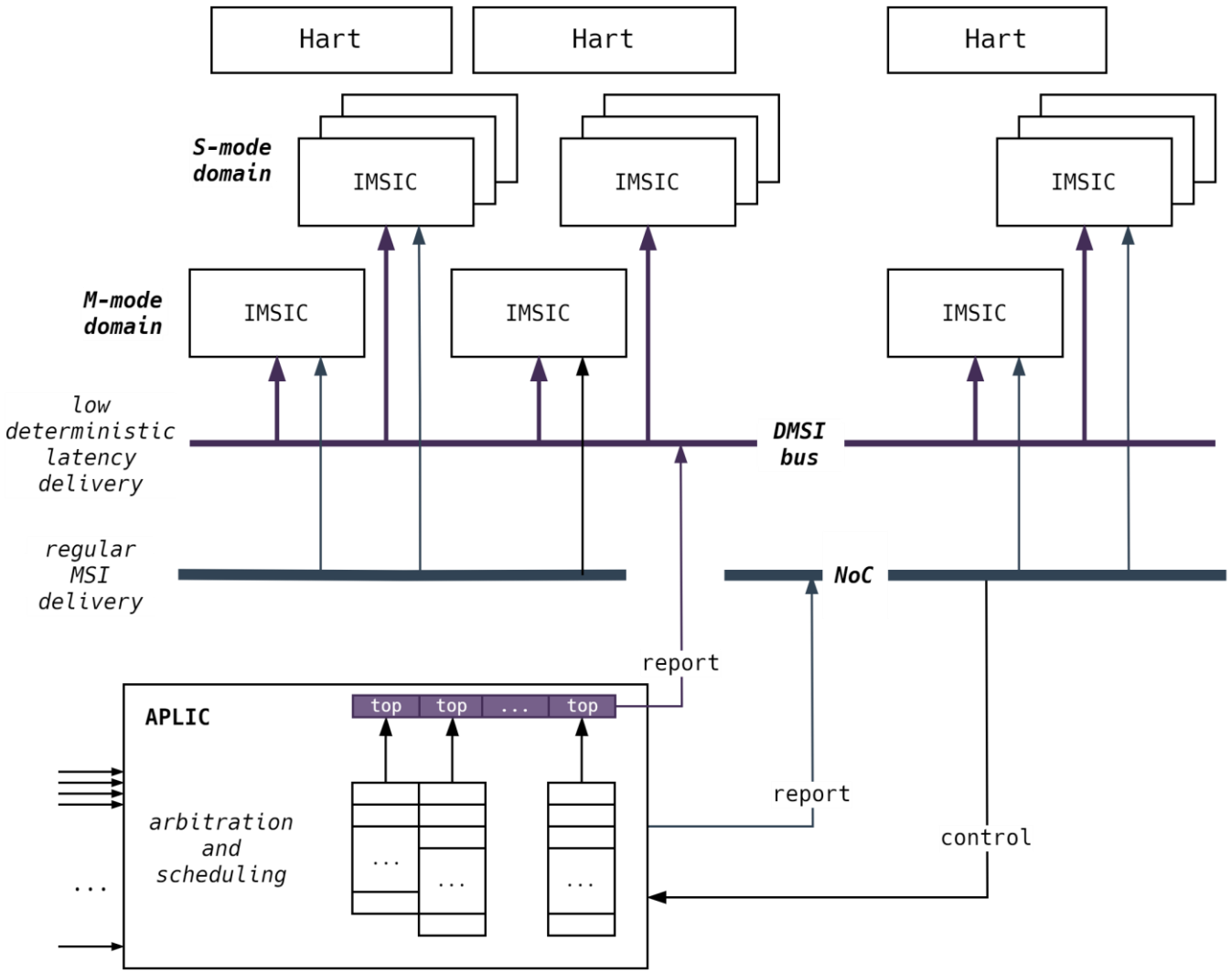
Real-Time Interrupt Delivery



- New *Direct Message Signaling Interrupt* (DMSI) delivery mode (optional)
- Configurable for each interrupt source at APLIC side
- Wide bandwidth, deterministic low latency DMSI bus
- Delivery prioritization by domain/target/priority
- DMSI cannot be initiated in software, regular MSI can be used for IPI

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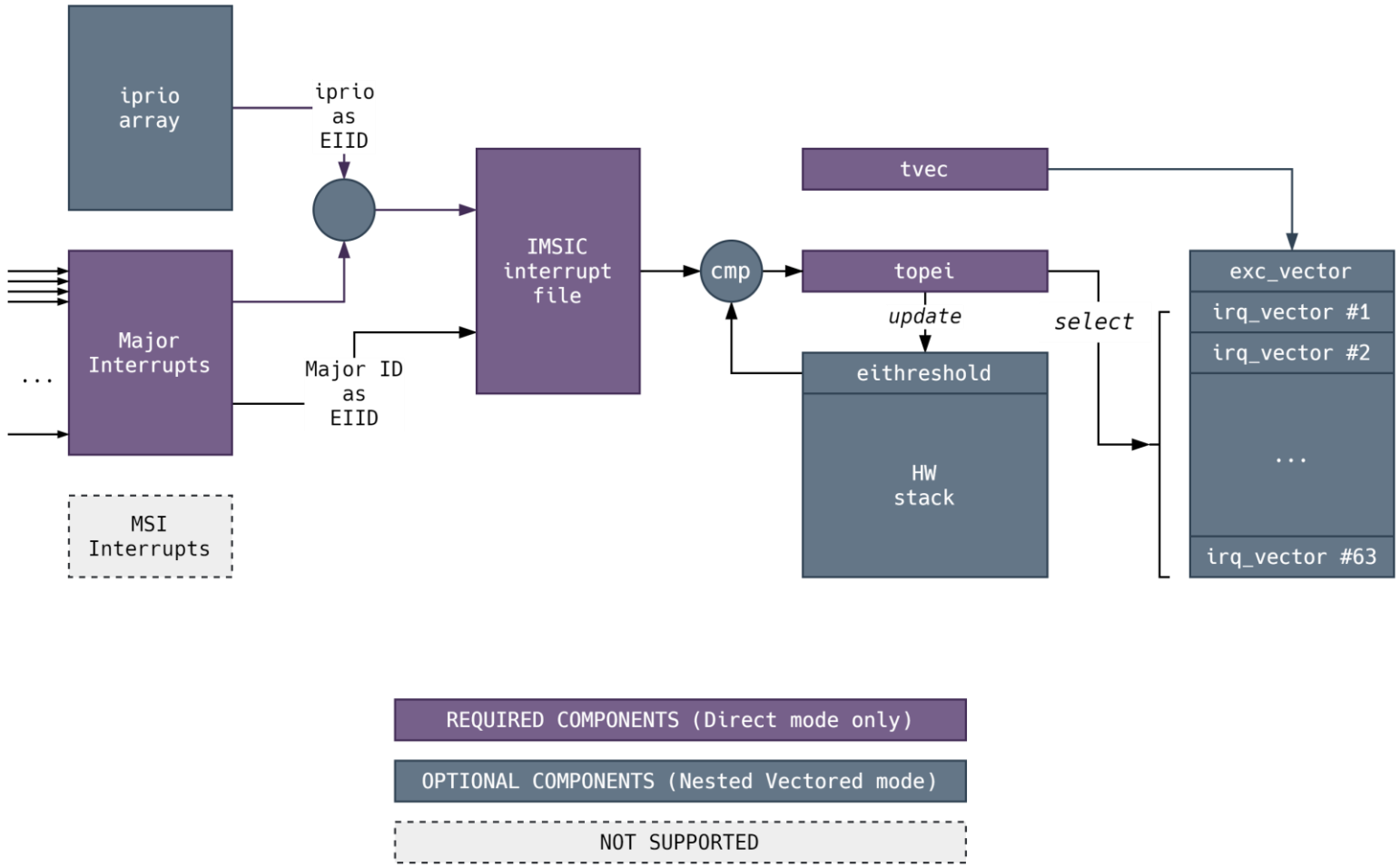
RISC-V Real-Time Interrupt Architecture

Single-core Configuration



- Core major interrupts routed via M-mode IMSIC
- Fixed or configurable major interrupt priorities (*iprio array*) are used as IMSIC EIIDs
- Optional interrupt threshold and *Nested Vectored* interrupt handling mode with up to 63 priority levels
- Backward compatibility with RISC-V Privileged ISA and AIA (incl. *Direct* and *Vectored* interrupt handling mode)

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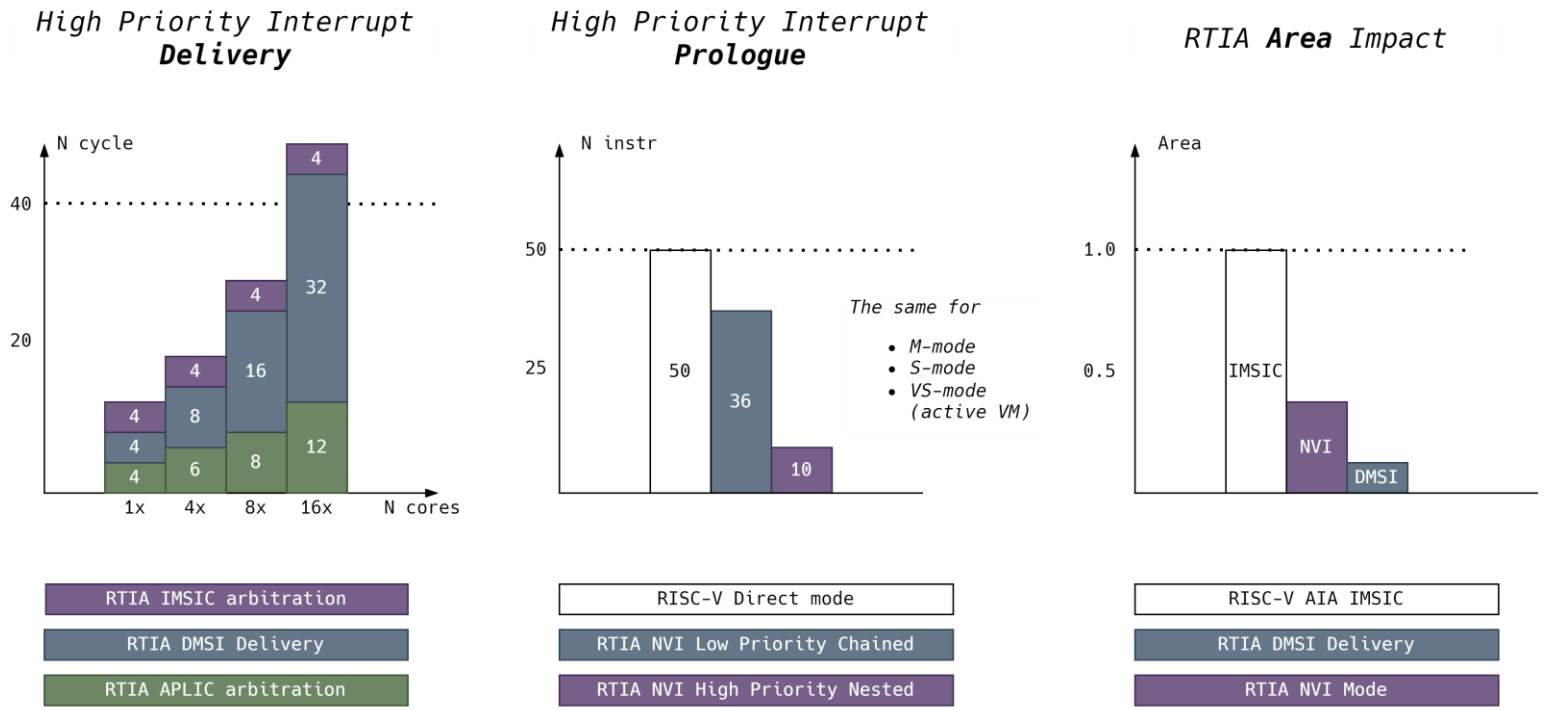
RISC-V Real-Time Interrupt Architecture

Latency and Area Impact



- Deterministic low latency interrupt delivery
- Low software overhead for interrupt prologue/epilogue
- Low/moderate hardware overhead to support nested vectored interrupts

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RISC-V Real-Time Interrupt Architecture

RTIA Extensions Development Status

- Completed
  - Synopsys RTIA Specification
  - Functional simulator
  - Instruction and cycle accurate simulator
  - Functional tests
  - Compiler support
  - Synopsys ARC-V RMX core IP (M/S/U-mode, no virtualization) RTL
- In progress
  - Synopsys ARC-V RHX core IP (incl. H-extension) RTL
  - Virtualization SW prototype (Type-1 hypervisor)
  - RTIA support in Linux kernel
  - OSS SW porting
- Plans
  - RISC-V RTIA Specification Proposal

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Thank you