LAUTERBACH
DEVELOPMENT TOOLS

RISC-V

Utilizing RISC-V Trace Standards for Efficient Bugfixing and Profiling

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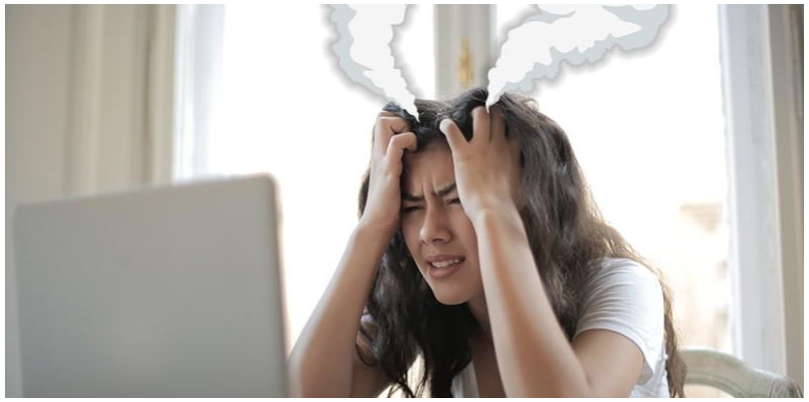
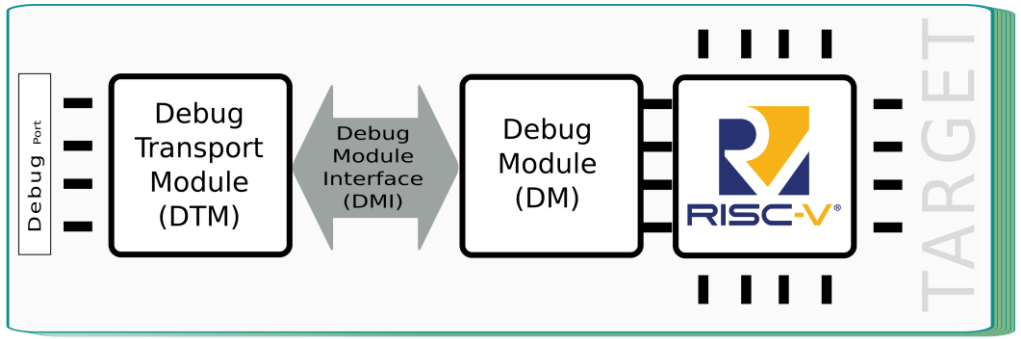
Challenges Embedded Developers are Facing Today

- Driven by market requirements, embedded systems and chip architectures are becoming more complex:
  - → More powerful processors of different architectures like RISC-V in different multicore configurations (SMP, AMP).
  - → Different operating systems such as Linux as a "rich operating system" , RTOS or an AUTOSAR variant in the automotive industry.
- Heterogeneous multicore architectures increase the requirements for bug fixing and thus for both pure debuggers and real-time trace.



RISC-V Debugging Made Easy

- „RISC-V External Debug Support“ Specification v1.0.0 incorporates everything needed for simple and complex debugging scenarios

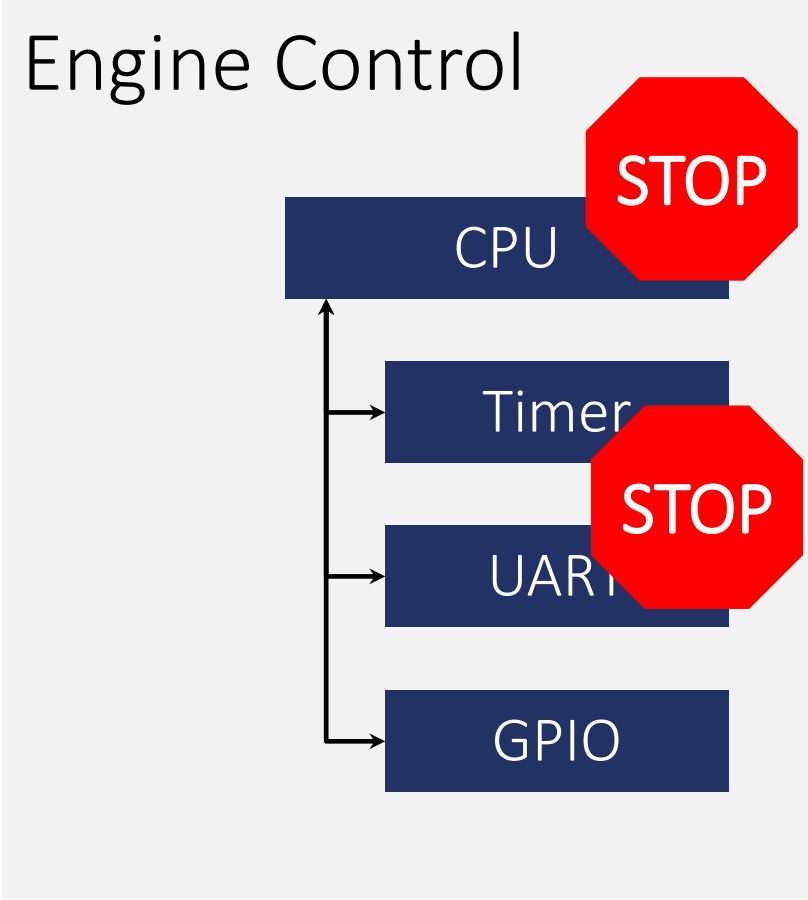


  - Great solution for simple and fairly complex RISC-V Systems

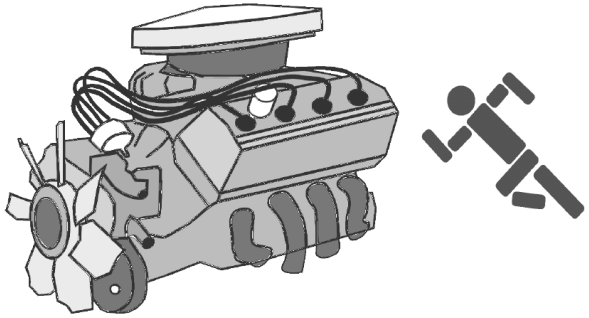
- Open to adaptions to support most complex and diverse SoCs
  - Flexible DTM designs make heterogeneous debugging easy
  - Several options to add peripheral IP such as Trace

From Debug to Trace

- We can freeze the core
- We might freeze also some peripherals
- But we can not freeze the surrounding

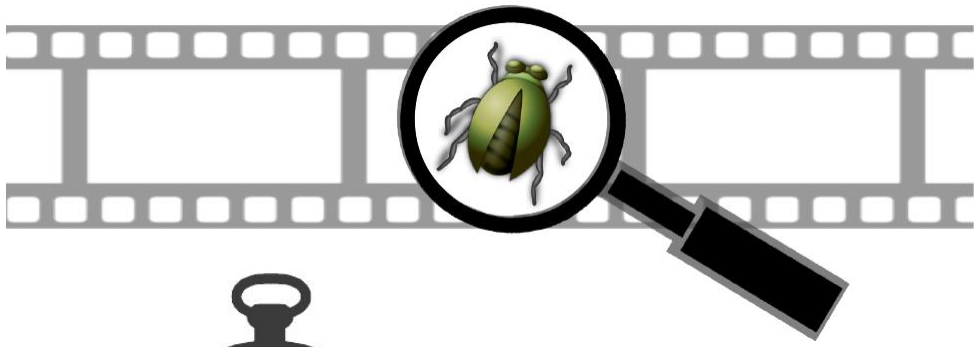


How can we still find bugs?



Trace Supplements Debugging

- Trace based debugging
  - Debug without stopping the CPU
  - Find bugs which appear only in real time



- Optimizing with timing measurements
  - Analyse the code performance of the application
  - Analyse outside events

- Qualification
  - Prove the meeting of real time requirements
  - Prove code coverage

RISC-V Trace Solutions

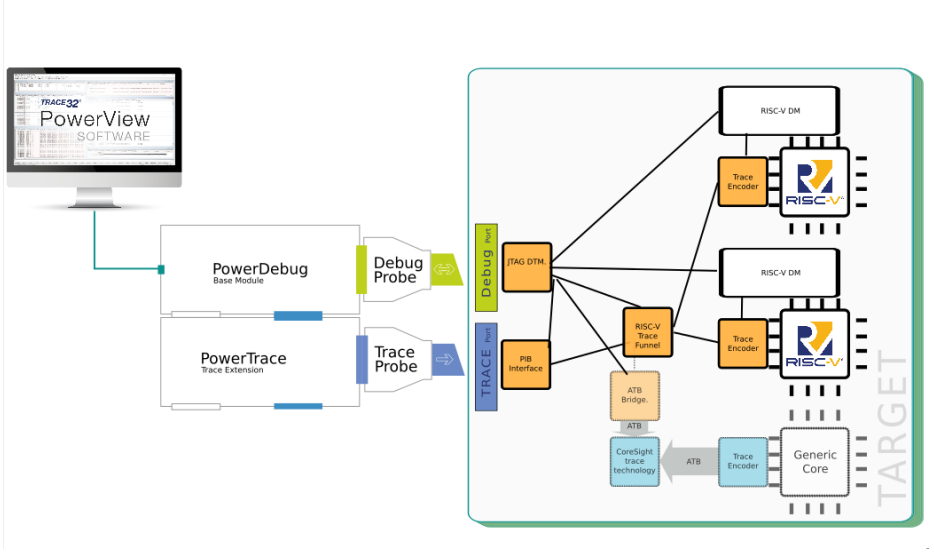
- Specifications for two RISC-V Trace Standards have been ratified recently
  - RISC-V E-Trace Standard
  - RISC-V N-Trace Standard

- Standards consist of different documents

	RISC-V N-Trace Specification	RISC-V E-Trace Specification	RISC-V Unformatted Trace Packet Encapsulation Specification	RISC-V Trace Control Interface Specification	RISC-V Trace Connectors Specification
RISC-V **N-Trace**	•			•	•
RISC-V **E-Trace**		•	•	•	•

RISC-V Trace Solutions

- RISC-V trace specifications are also suitable for heterogeneous systems
- Flexible ways to access the trace component‘s configuration registers via System Bus Access, DMI, message passing networks, …
- Filters to limit trace usage
- Transportability via other trace infrastructure such as CoreSight ATB
- Lauterbach supports the latest versions of the E- and N-Trace specifications in various implementations
- We will discuss this later in more detail



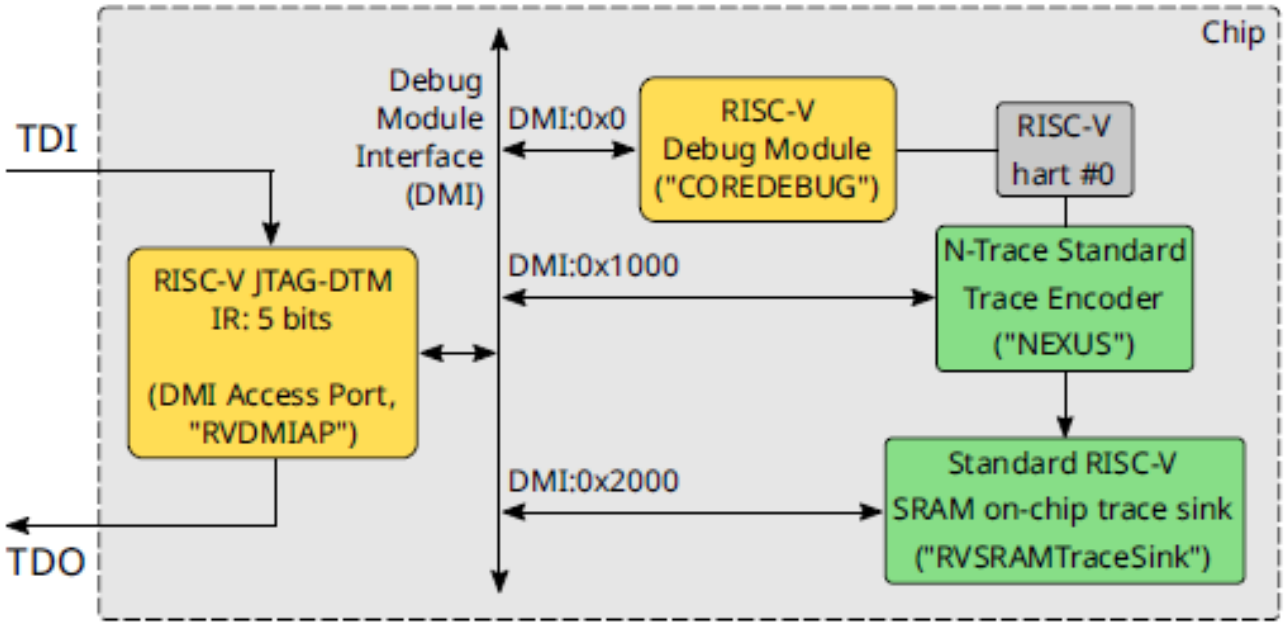
Compare RISC-V Trace Specifications

- Currently no assessment as to which is better
  - Different optimization mechanisms and protocol characteristics
  - Efficiency depends how good chip, application and trace protocol work together

N-Trace	E-Trace
Instruction Trace	Instruction + Data Trace
Inferable Jump Optimization	Inferable Jump Optimization
Implicit Return Optimization (in different modes)	Implicit Return Optimization
Repeated History Optimization	Address Optimization
Virtual Address Optimization	Implicit Exception Optimization
	Branch Prediction Optimization
	Jump Target Cache Optimization

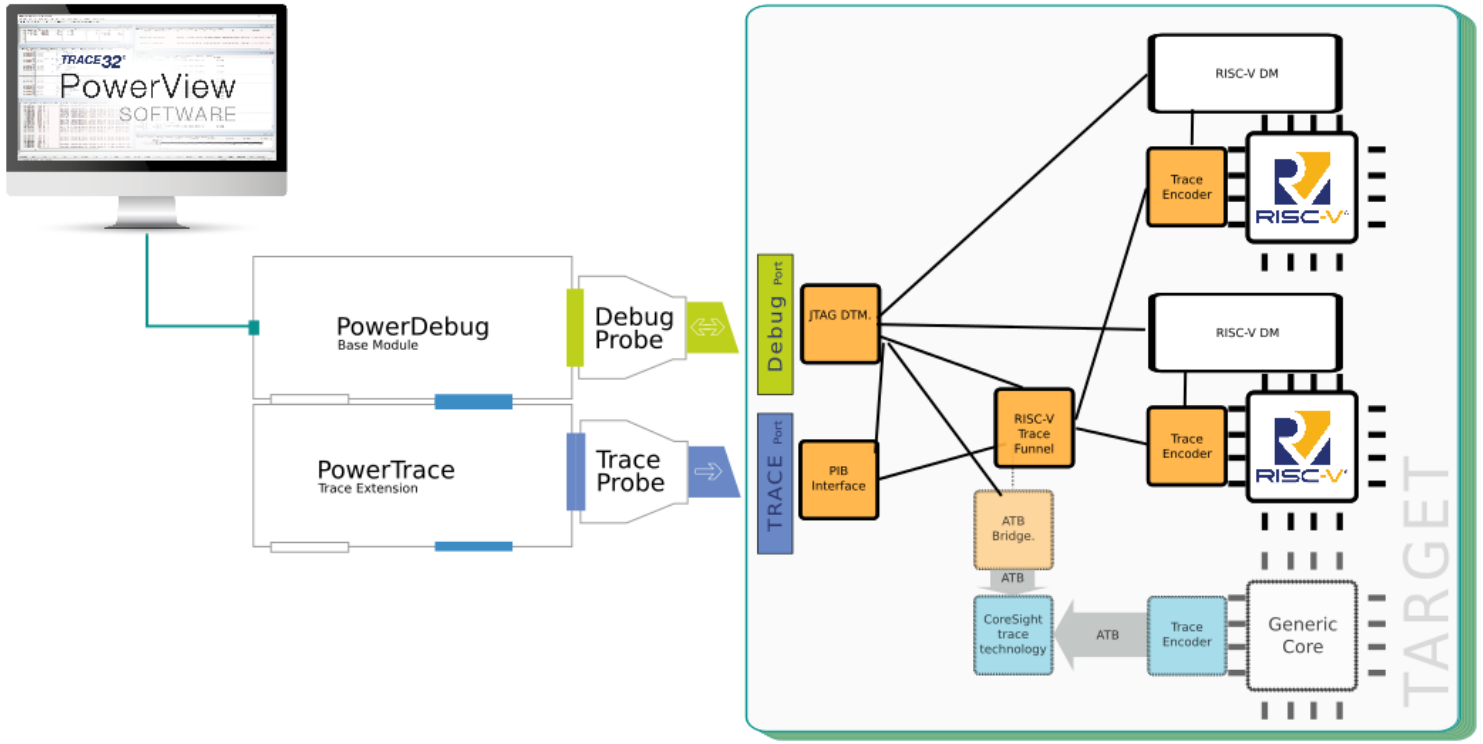
Case Study: Simple RISC-V Trace

- Small embedded RISC-V controller
- Simple and easy to use trace infrastructure



Case Study: Heterogeneous RISC-V Trace

- More complex system with RISC-V and other cores
- Fits to all possible tracing requirements



Last but not Least: Lauterbach is **Always** at the Forefront of RISC-V Technology

Lauterbach Supports Infineon's Automotive RISC-V Virtual Prototype

Publishing Date: March 7, 2025

Lauterbach and Kernkonzept enable Virtualized RISC-V Systems

Publishing Date: October 14, 2024

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Summary

- Chips are getting more and more complex and implement a growing number of RISC-V cores in different (heterogeneous) multicore configurations (SMP, AMP).
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beg
- Lauterbach's modular TRACE32 system covers all debug and trace requirements for any RISC-V-based chip today – find your solution easily here: https://www.lauterbach.com/supported-platforms/architectures/risc-v

For more details download our Whitepaper

„Debugging of RISC-V-Based Chips Made Easy “:

https://www2.lauterbach.com/download/pdf/white-paper/whitepaper-debugging-risc-v-based-chips-made-easy.pdf

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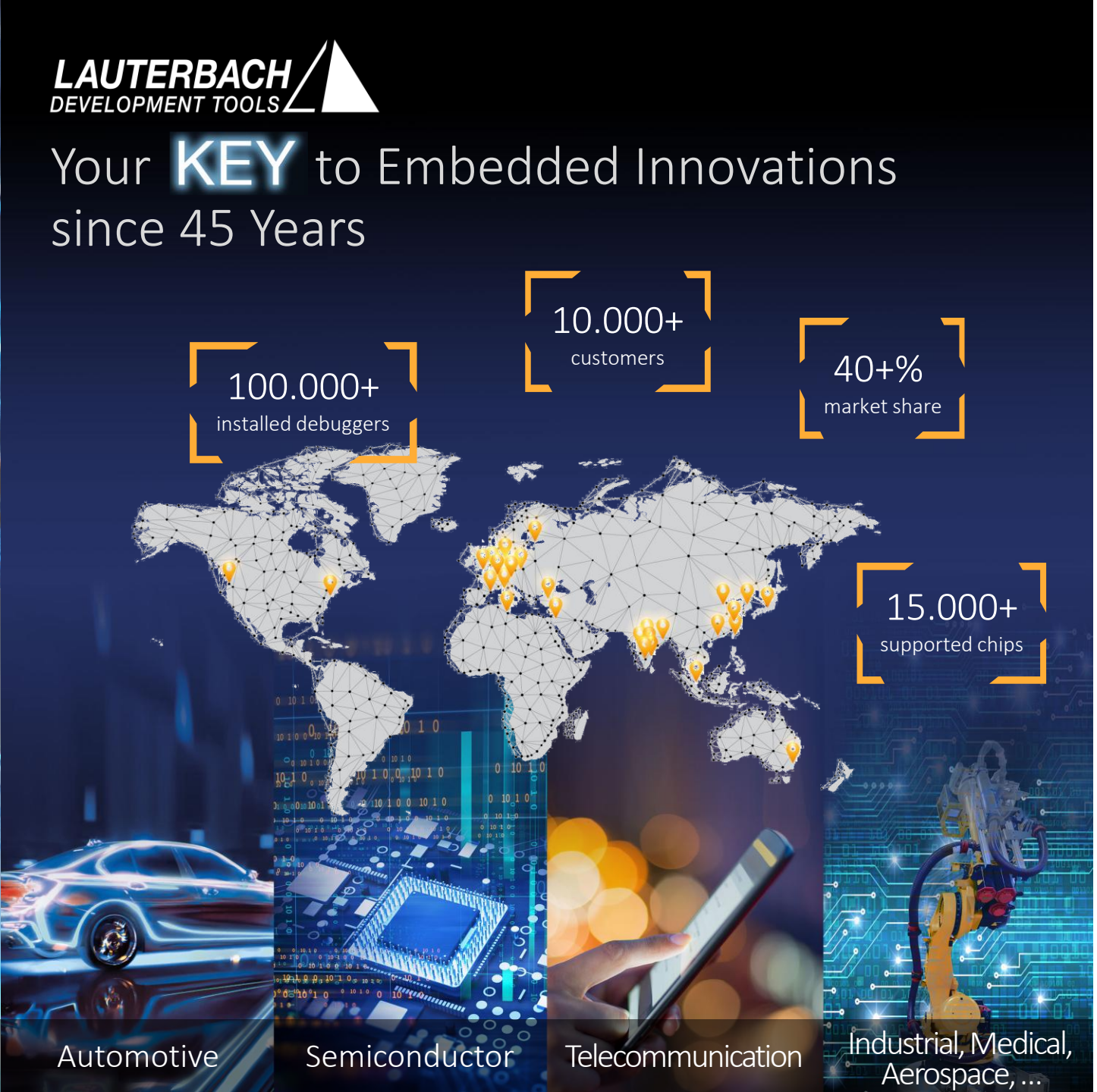

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Live-Demo & Discussion at Lauterbach Booth

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QUESTIONS?