# Getting towards first-time RISC-V silicon with automated end-to-end formal

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axiomise®
predictable formal verification

# formalISA®

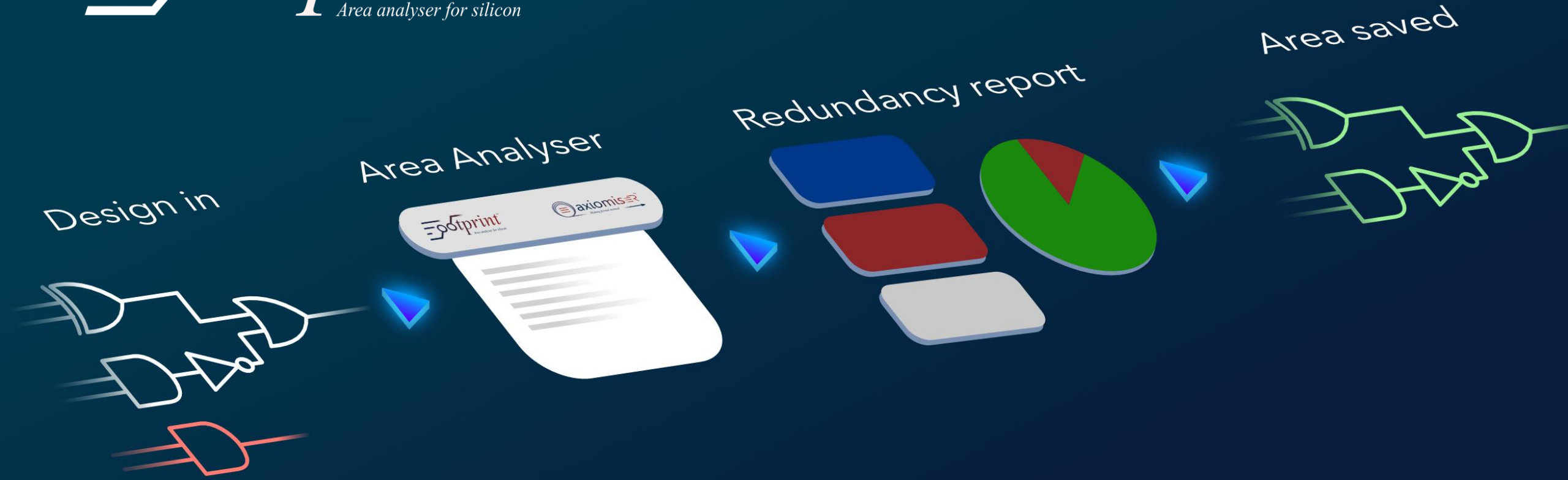
*Making formal normal for RISC-V*


Accelerating debug and sign-off for custom designs using exhaustive formal

axiomise®
*predictable formal verification*

# Footprint®

*Area analyser for silicon*

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PUSH BUTTON

PROOFS, BUGS, COVERAGE

RESULTS

Footprint®
Area analyser for silicon

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