RISC-V Europe Summit 2025 Launchpad
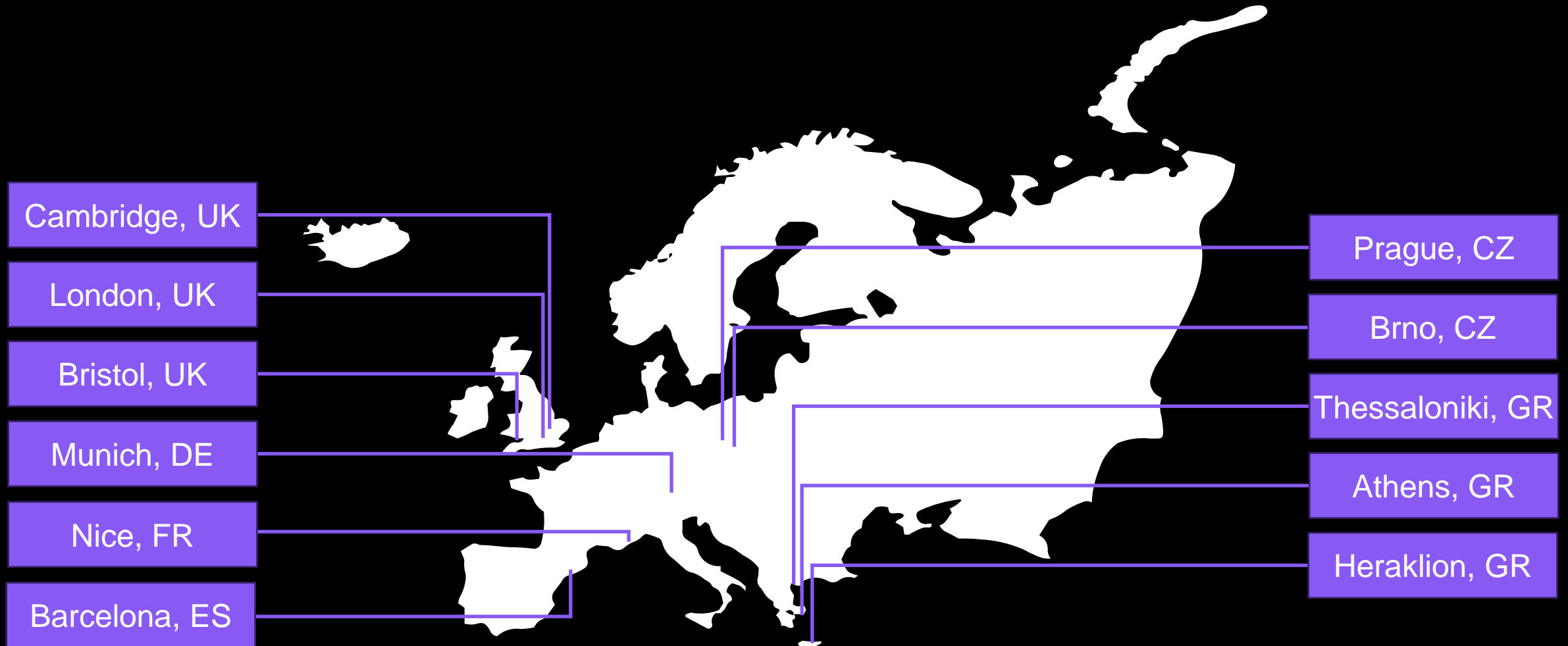
What's new at Codasip?

Codasip

Peter Shields

RISC-V Europe Summit, Paris, May 2025
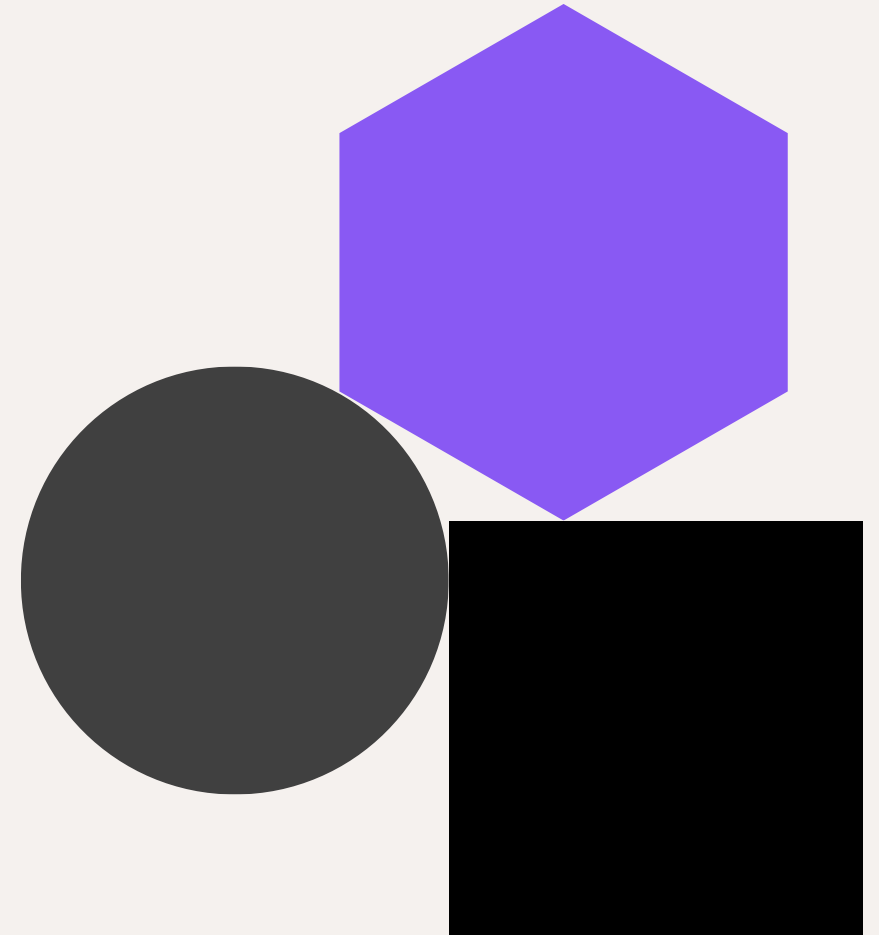
Codasip

Cambridge, UK

London, UK

Bristol, UK

Munich, DE

Nice, FR

Barcelona, ES

Prague, CZ

Brno, CZ

Thessaloniki, GR

Athens, GR

Heraklion, GR

Codasip

1. Customizable RISC-V cores

   - L150 low-area/power core

   - RISC-V port of CMSIS (see the demo)

2. CHERI enabled RISC-V cores

   - CHERI-Linux (see the demo)

3. Functional Safety RISC-V cores

   - L730 (ASIL-B & ASIL-D)

4. Studio Fusion
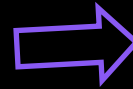
Codasip

1. Customizable RISC-V cores

   • L150 low-area/power core

   • RISC-V port of CMSIS (see the demo)

2. **CHERI** enabled RISC-V cores

   • CHERI-Linux (see the demo)

Customizable HPC

dare

3. Functional Safety RISC-V cores

   • L730 (ASIL-B & ASIL-D)

4. Studio Fusion

Codasip

Posters

- Customized RISC-V in a simple game console
- Codasip's X730 core, the world's first commercially available CHERI RISC-V Application Core
- Efficient system level support for CHERI Capabilities
- CHERI performance optimization
- Standardizing CHERI-RISC-V, CHERI TG specification and status update

Demo theater

- Using CMSIS for simplified migration to RISC-V

Panel session

- Accelerating Automotive Innovation with RISC-V

Exhibition Area

- CHERI-Linux demo
- CMSIS porting and acceleration