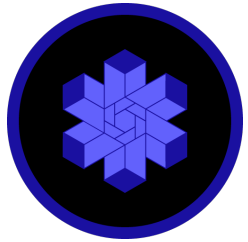
# From RISC-V with AI to AI with RISC-V

Volker Politz
Chief Sales Officer
May 2025

In Order Core

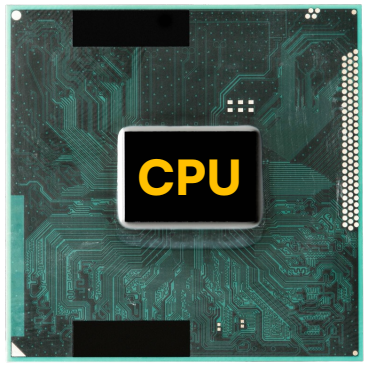
OOO Core



OOO Vector Unit

Tensor Unit

# We started with a look at CPU...




**Market Needs**
- DMIPS / SPECint
- Cash Management
- Memory Bandwidth

64-Bit
RISC-V CPU

**More Data**
- Big Data Movement
- Vectorized Data Bases
- Complex AI tasks

Vector Unit

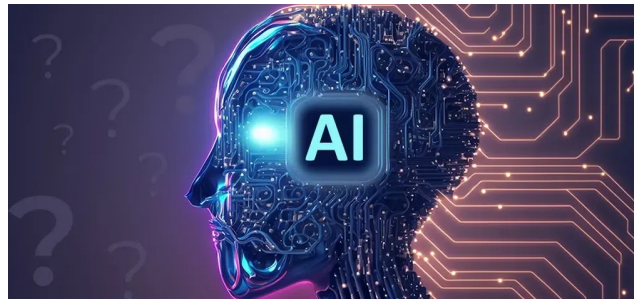
**Even More Data**
- Memory Wall
- Cash Misses

Gazzillion
Misses™

**AI algorithm enablement**
- Matrix Multiplications

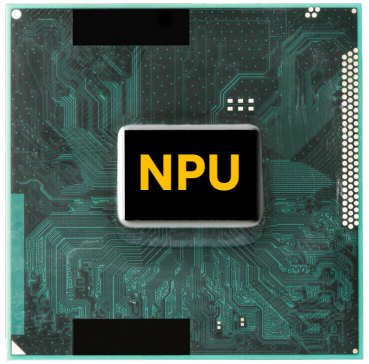
Tensor Unit

Do More with CPU !

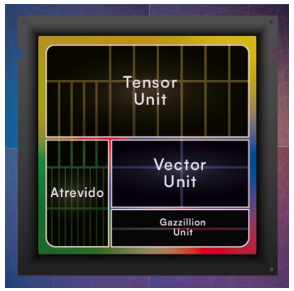



semidynamics

# ...and we saw a RISC-V enabled NPU !




**Market Needs**
- TOPS
- Token/Sec

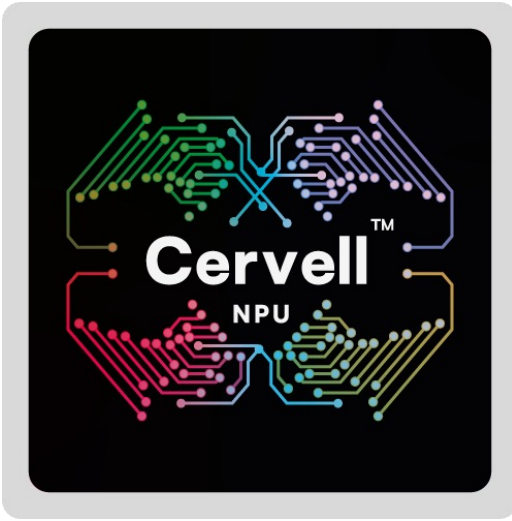



**Single RISC-V ISA AI compute element**

mxnet PyTorch Cognitive Toolkit
K Caffe2 TensorFlow Hugging Face

ONNX

**Aliado SDK**
**ONNX Support**




**NPU**
**RISC-V ISA**

**Delivering the Risc-V ISA benefits to NPU markets”**

semidynamics

# Thank you

semidynamics