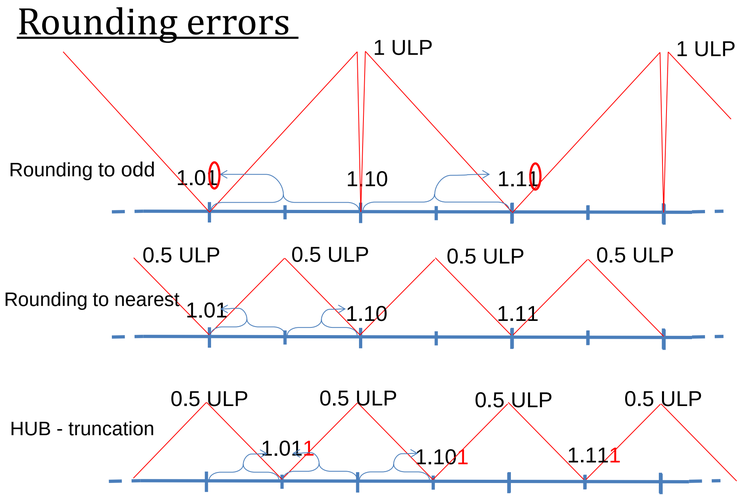
FPHUB-RISCV: HUB Floating-Point Unit in RISC-V Platform -- Format definition

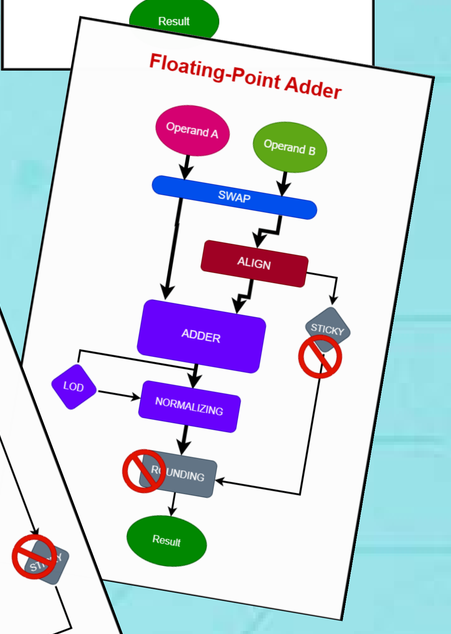
Previous Research

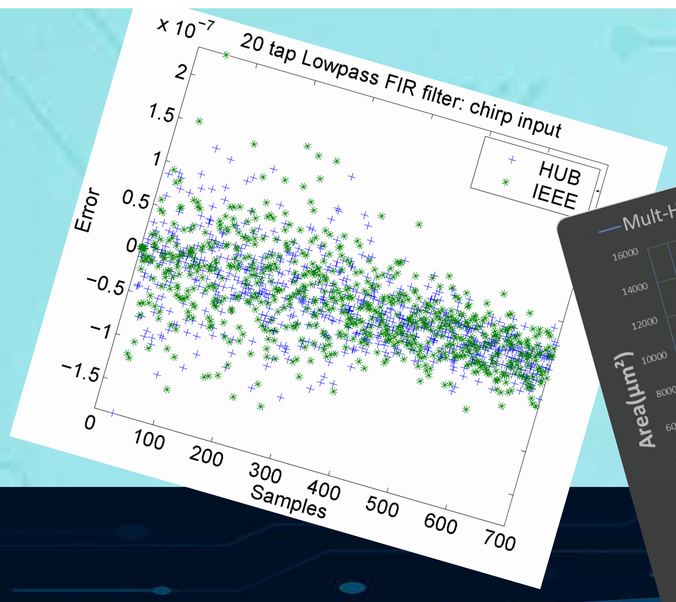
Rounding errors

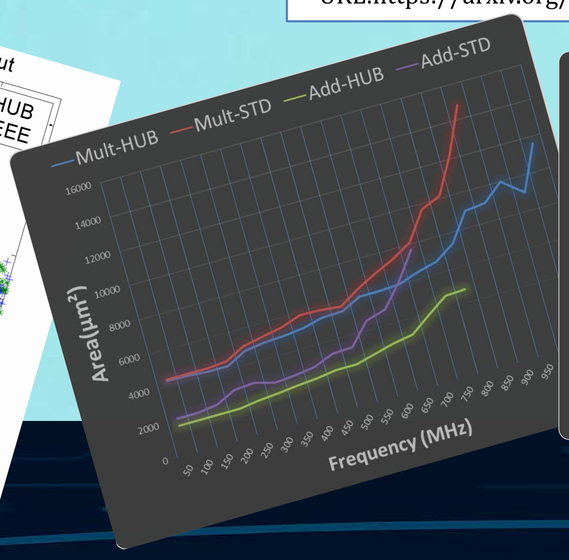


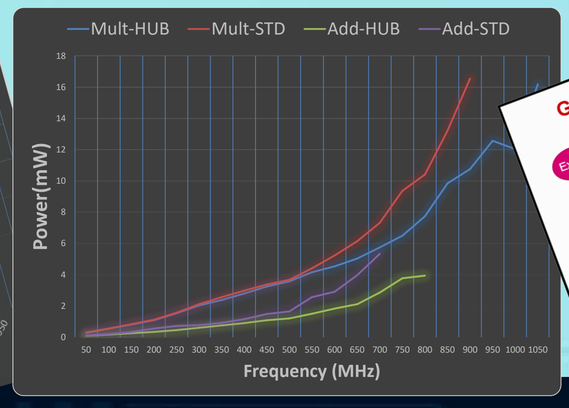
Publications

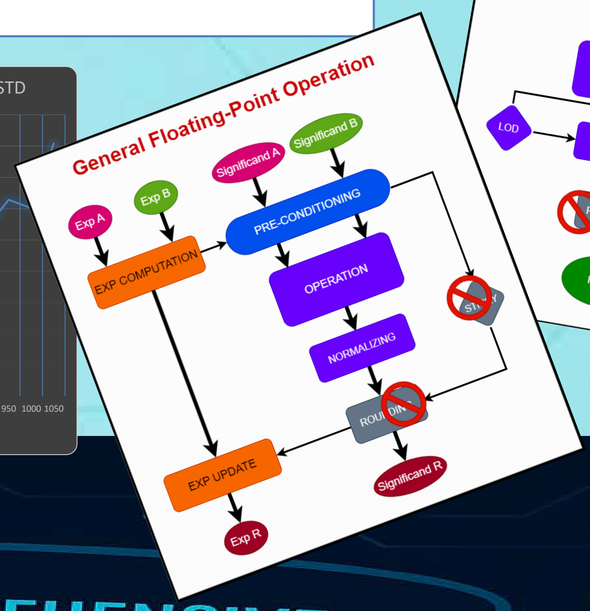
- J. Hormigo, J. Villalba-Moreno and S. Gonzalez-Navarro, "Floating–Point Fused Multiply–Add under HUB Format," 2020 IEEE 27th Symposium on Computer Arithmetic (ARITH), Portland, OR, USA, 2020, pp. 1-8, doi: 10.1109/ARITH48897.2020.00010.
- J. Villalba-Moreno, J. Hormigo and S. González-Navarro, "Unbiased Rounding for HUB Floating-Point Addition," in IEEE Transactions on Computers, vol. 67, no. 9, pp. 1359-1365, 1 Sept. 2018, doi: 10.1109/TC.2018.2807429.
- J. Villalba-Moreno and J. Hormigo, "Floating Point Square Root under HUB Format," 2017 IEEE International Conference on Computer Design (ICCD), Boston, MA, USA, 2017, pp. 447-454, doi: 10.1109/ICCD.2017.79
- J. Hormigo and J. Villalba, "HUB Floating Point for Improving FPGA Implementations of DSP Applications," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 64, no. 3, pp. 319-323, March 2017, doi: 10.1109/TCSII.2016.2563798.
- J. Villalba-Moreno, "Digit Recurrence Floating-Point Division under HUB Format," 2016 IEEE 23nd Symposium on Computer Arithmetic (ARITH), Silicon Valley, CA, USA, 2016, pp. 79-86, doi: 10.1109/ARITH.2016.17.
- J. Hormigo and J. Villalba, "Measuring Improvement When Using HUB Formats to Implement Floating-Point Systems Under Round-to-Nearest," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 24, no. 6, pp. 2369-2377, June 2016, doi: 10.1109/TVLSI.2015.2502318.
- J. Hormigo and J. Villalba, "New Formats for Computing with Real-Numbers under Round-to-Nearest," in IEEE Transactions on Computers, vol. 65, no. 7, pp. 2158-2168, 1 July 2016, doi: 10.1109/TC.2015.2479623.
- Gerardo Bandera et al. Floating Point HUB Adder for RISC-V Sargantana Processor. 2023. URL:https://arxiv.org/abs/2401.09464.











ROBUST TESTING · COMPREHENSIVE DOCUMENTATION

SOFTWARE SIMULATION LIBRARY

HUB-FP FORMAT DEFINITION

- Mantissa has the form $1.M_X1$, where M_X is the fractional part and the only explicit.
- The bias of the exponent is set to 2^{n-1} instead of $2^{n-1}-1$(IEEE)
- Rounding is always Round-to-nearest, implemented by truncation
- No use of NaN or subnormals (flushed to zero)
- Special cases: zero, one, and infinity; all with sign.

RIGOROUS TESTING

- Extensive HDL simulation
- Software simulation of typical applications
- Hardware emulation in FPGA
- Performance evaluation

SEEKING COLABORATION

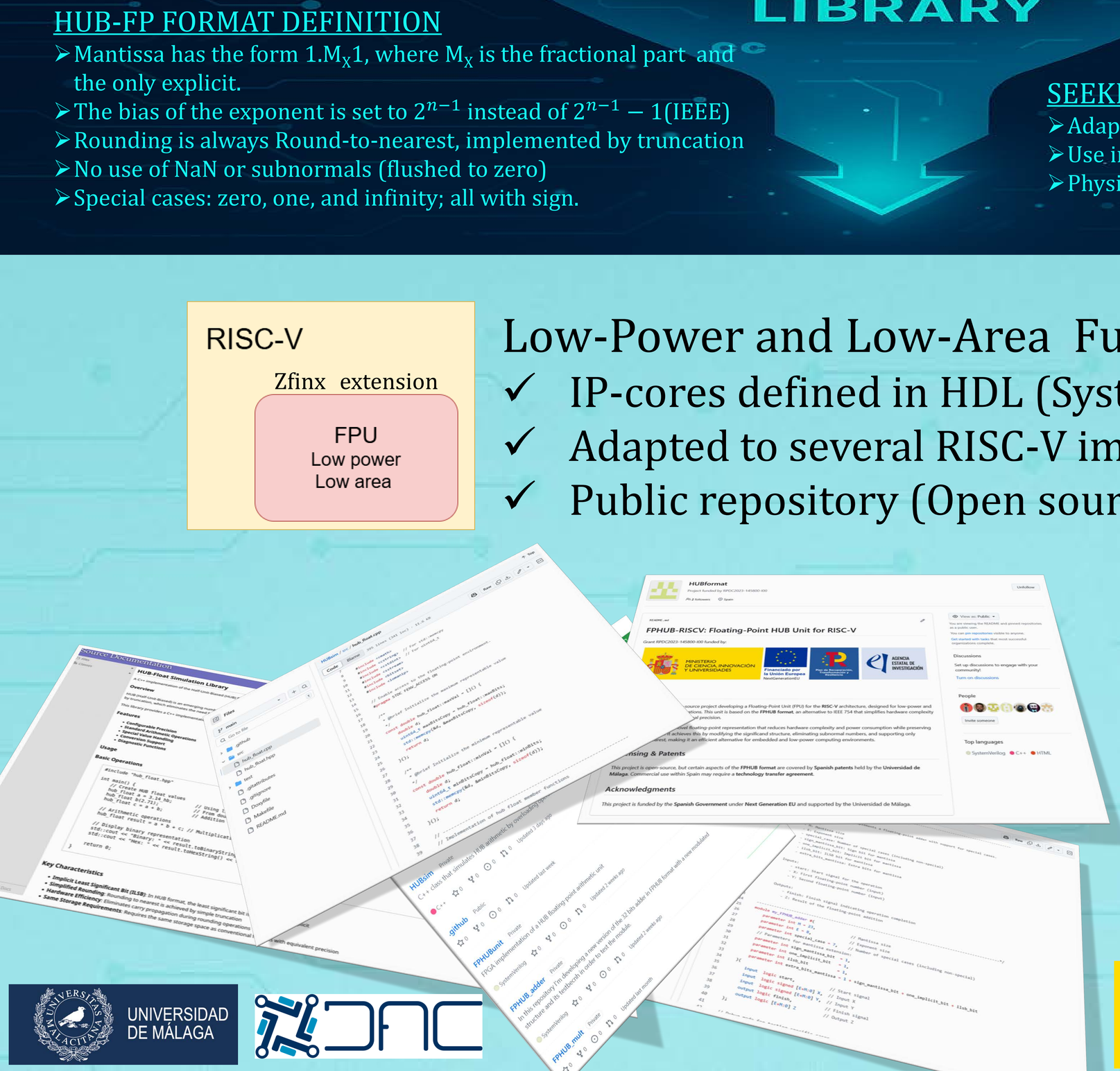
- Adaptation to specific RISC-V implementation
- Use in real applications
- Physical implementation

RISC-V
Zfinx extension

FPU
Low power
Low area

Low-Power and Low-Area Full Floating-Point Unit:

- ✓ IP-cores defined in HDL (SystemVerilog)
- ✓ Adapted to several RISC-V implementations
- ✓ Public repository (Open source)



Public Repository: https://github.com/HUBformat

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