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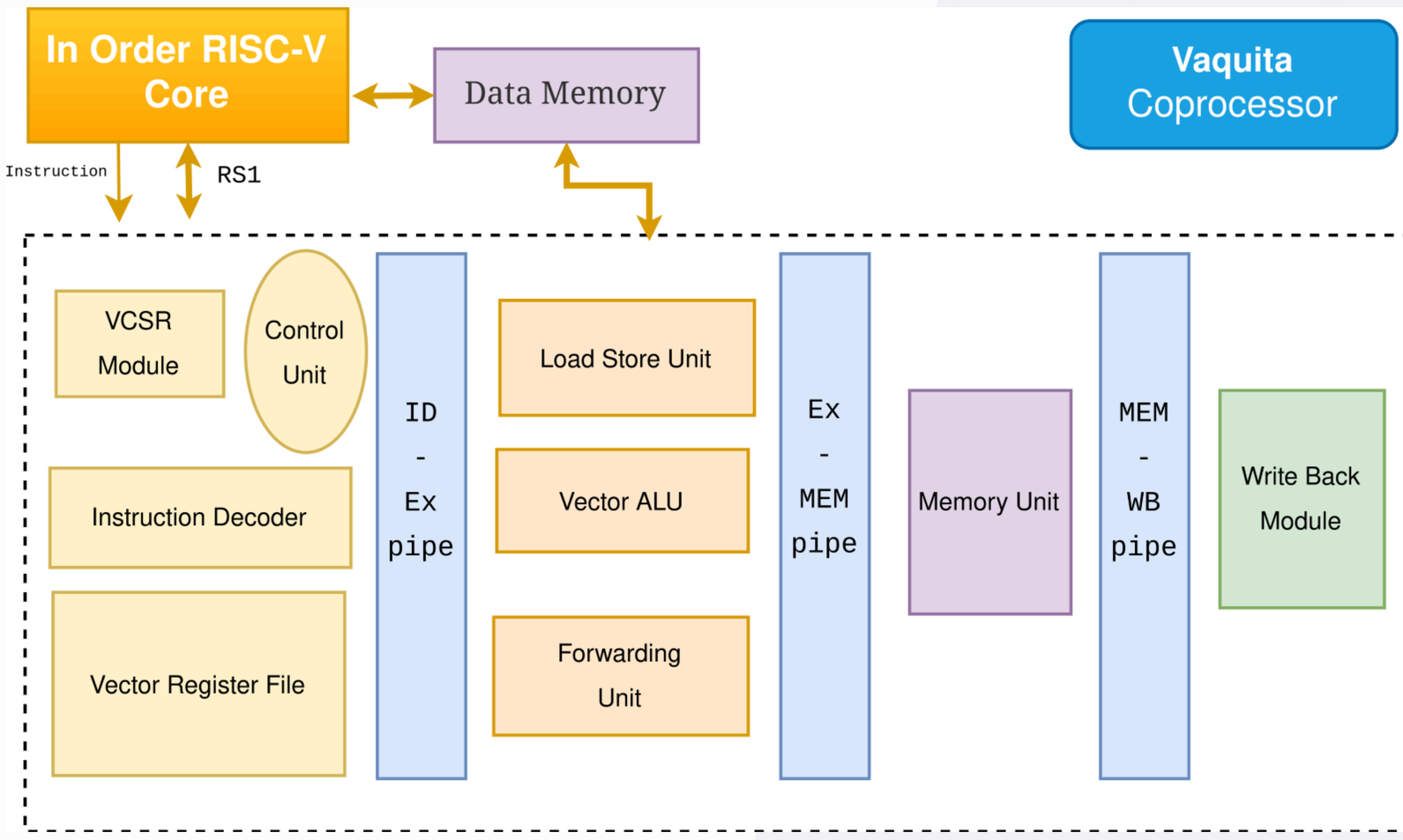
Vaquita: A Portable Four Stage Pipeline RISC-V Vector Co Processor

A CHISEL-based RISC-V Vector (RVV) v1.0 co-processor featuring a 4-stage optimized vector pipeline for high-performance vector processing. The design ensures high throughput, low latency, and efficient data hazard resolution, seamlessly integrating with diverse RISC-V systems through a plug-and-play interface.

Features

Riscv Vector 1.0

- Implements RVV v1.0 for scalable SIMD processing.
- Supports SEW = 8, 16, 32 and LMUL>=1
- configurable VLEN



Modular 4-Stage Pipeline Design

- **ID (Instruction Decode):** Analyzes vector instructions, extracting opcode and operands
- **EX (Execution):** Parallel Vector ALU with EEW-specific lanes and forwarding logic.
- **MEM (Memory):** Load/store vector elements using memory interface.
- **WB (Write-Back):** Writes computed results to vector register file.

Application Domains

- AI/ML accelerators (e.g., vectorized inference)
- Signal and image processing
- Scientific computing with SIMD workloads

Dynamic Lane Allocation

- Number of ALU lanes is determined based on VLEN and SEW.
- Supports ELEN = 32 bits
- Implements data hazard detection for RAW dependencies.
- Forwarding Unit provides intermediate results to subsequent instructions to prevent stalls.
- Maintains pipeline integrity and throughput.

Future Enhancements

- Improve memory access patterns.
- Add the remaining part of the vector extension.
- Compare Vaquita with other vector co-processors (e.g., Hwacha, ARA).

Source Code!

Table 1: PPA Metrics for the Proposed Design

Design Compiler	Synopsis
Technology	FreePDK45
Frequency	1GHz
Total Area	0.421mm^2
Total Power	50.2517mW