XiangShan Kunminghu V2: Architectural Innovations and Ecosystem Development of an Open-Source High-Performance RISC-V Processor

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Abstract

XiangShan Kunminghu V2, an open-source RISC-V processor achieving 45 SPEC06 at 3GHz, implements RVA23 Profile with hardware virtualization and 1024-bit vector processingin a single instruction, supported by an agile development ecosystem attracting 6k GitHub stars. The industry-academia co-design mechanism through BOSC innovation consortium has enabled 24 industrial partnerships, providing open source and shared base technical support for advanced computing ecosystem.

Background and Motivation

The semiconductor industry is undergoing a paradigm shift towards open-source collaboration, with RISC-V emerging as a transformative force in processor architecture. This open ISA standard, recognized by MIT Technology Review's 2023 Top 10 Breakthrough Technologies, has catalyzed a new era of modular and customizable chip design. Within this evolving landscape, two critical challenges persist in open-source processor development:

- **Performance Limitations**: Prior to XiangShan, no open-source RISC-V implementation exceeded 10 SPEC06 points, creating an adoption barrier for performance-sensitive applications
- **Configurability Deficit**: Industrial applications require domain-specific optimizations that existing academic prototypes couldn't deliver through parameterized configurations

XiangShan's development directly addresses these challenges through three strategic innovations. First, its open-source microarchitecture reveals industrial-grade design techniques previously guarded as trade secrets. Second, the configurable pipeline architecture supports hundred of tunable parameters ranging from cache hierarchy to execution width. Third, the co-development model through BOSC innovation consortium bridges the academia-industry gap, enabling continuous performance scaling across three architectural generations.

This tripartite approach has propelled XiangShan Kunminghu V2 to achieve 45 SPEC06 at 3GHz - a 6.4× improvement over its initial 2019 implementation while maintaining full design transparency. The project's GitHub traction (6k stars) reflects growing industry recognition of open-source hardware's potential to reshape traditional design paradigms.

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Kunminghu V2 Architecture

Architectural Overview

The third-generation Kunminghu architecture represents a quantum leap in open-source processor design. Operating at 3GHz with 45 SPEC06 score, it features a completely rearchitected multi-stage pipeline supporting simultaneous multithreading. Key innovations include a post-issue register read design reducing pipeline stalls with a smaller area, and CHI protocol integration enabling seamless scaling to 64-core configurations.

RVA23 Profile Implementation

Compliance with the latest RISC-V standards positions Kunming Lake as a cloud-ready solution. Beyond mandatory extensions like H-extension (virtualization) and V-extension (vector processing), the implementation also includes optional security features like compare-and-swap (Zacas) and half-precision floating point (Zfh and Zvfh).

Virtualization Acceleration

Hardware-assisted virtualization employs a three-layer approach:

- **CPU**: Nested virtualization via 4 privilege levels
- **Memory**: Two-stage address translation with 48-bit physical addressing

- **I/O**: IOMMU supporting direct communication between VMs and devices

This hardware-assisted virtualization architecture can significantly reduce hypervisor overhead which is necessary for cloud computing.

Vector Processing Unit

With the help of the V-extension, Kunminghu V2 has gained the capability for single-instruction multiple-data (SIMD) processing. The 128-bit vector registers and the maximum lmul configuration of 8 allow a single instruction to process up to 1024 bits of data, enabling practical AI inference workloads. Benchmark tests show 24.4% improvement in bioinformatics applications (hmmer).

Agile Development Ecosystem

The XiangShan infrastructure revolutionizes processor design through three core components. For example, the Xfuzz framework generates targeted test cases using genetic algorithms, improving bug detection rate. The TIP/TIE toolkit enables cycle-accurate performance analysis at instruction granularity, crucial for identifying pipeline bottlenecks. The continuous integration pipelines also automate regression testing across 1,200+ test cases, ensuring architectural stability during rapid iterations.

Open-Source Collaboration

Community engagement forms the cornerstone of XiangShan's success. With more than 6k GitHub stars and 730 forks, the project has cultivated an active developer base. The annual Developer Conference attracts hundred of participants, and academic collaborations have yielded 20+ research papers with architectural innovations adopted into the mainline codebase.

Industrial Co-Design Framework

The BOSC innovation consortium establishes a three-stage productization process:

1. Academic prototype validation
2. Industrial-grade hardening
3. Commercial deployment

Through 90+ technical exchanges and 350+ validation reports, industrial partners contribute critical expertise in reliability engineering and automotive-grade certification.

Conclusion

XiangShan demonstrates that open-source processor development can achieve commercial-grade performance while fostering innovation. With a faster design iterations and performance rivaling ARM Neoverse N2, the project establishes a new paradigm for collaborative hardware development.