北京开源芯片研究院
BEIJING INSTITUTE OF OPEN SOURCE CHIP

XIANGSHAN

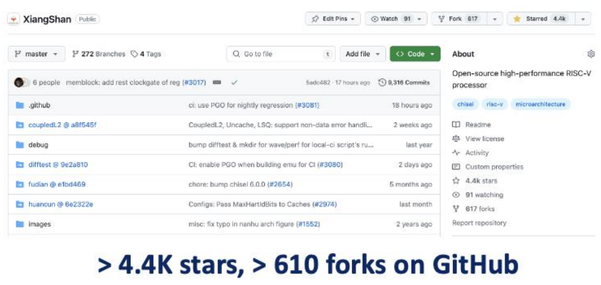
XiangShan Kunminghu V2: Architectural and Ecosystem Development of an Open-Source High-Performance RISC-V Processor

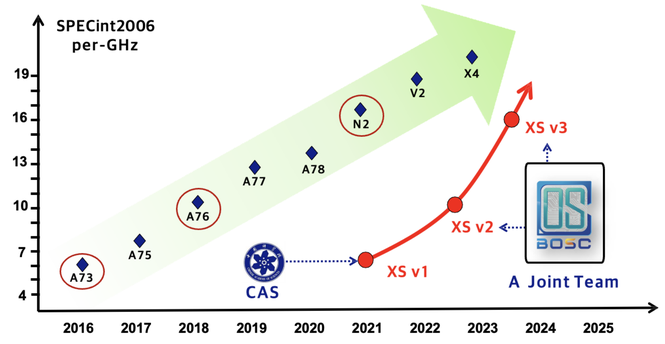
Haojin Tang, Haoyuan Feng and Yungang Bao
State Key Lab of Processors, Institute of Computing Technology, Chinese Academy of Sciences
Beijing Institute of Open-Source Chip

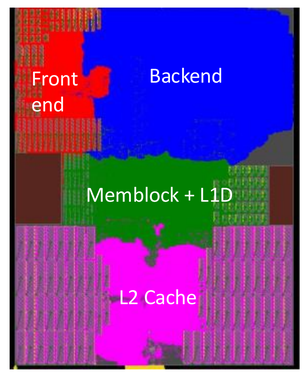
XiangShan Overview

XiangShan is an **open-source high-performance RISC-V processor** project introduced in 2020, aiming to establish a leading platform with end-to-end **agile development flows and tools** for commercial and research applications.

L1: OPEN ISA
L2: OPEN Design/Implementation
L3: OPEN Framework/Tools







Building upon the success of the first generation Yanqihu and the second generation Nanhu, the third generation Kunminghu has completed its RTL design and is ready for tape-out. The latest version of XiangShan, Kunminghu V2, achieves a normalized score of **45 at 3GHz on SPECint 2006**, with the performance competitive in the industry.

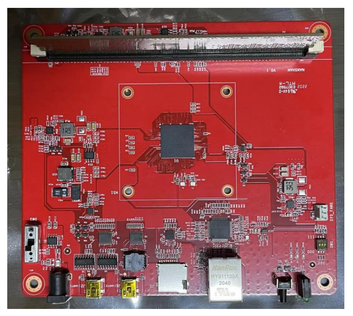
Highlights in XiangShan Kunminghu V2

- **Functional Enhancement**
  - RVA23 Compatible
  - CHI/TileLink Interconnection
- **Performance Exploration**
  - 1.5x IPC of XS Gen2, 3GHz
  - Multi-level composite prefetchers
  - Calibrated performance model
- **Functional Verification**
  - Hierarchical verification flow
  - Industrial-grade verification process

SPECint 2006 est. @ 3GHz		SPECfp 2006 est. @ 3GHz	
400.perlbench	38.1	410.bwaves	67.07
401.bzip2	25.53	416.gamess	42.95
403.gcc	47.17	433.milc	45.29
429.mcf	58.86	434.zeusmp	56.75
445.gobmk	30.3	435.gromacs	37.44
456.hmmer	40.79	436.cactusADM	49.3
458.sjeng	30.22	437.leslie3d	45.29
462.libquantum	124.56	444.namd	34.65
464.h264ref	57.72	447.dealII	74.37
471.omnetpp	40.11	450.soplex	54.63
473.astar	29.14	453.povray	54.95
483.xalancbmk	73.25	454.Calculix	18.33
GEOMEAN	**44.61**	459.GemsFDTD	40.22
SimPoint Based Sampling GCC 12 -O3, RV64GCB, jemalloc DRAMsim3 DDR4 @ 3200MHz		465.tonto	37.99
		470.lbm	102.47
		481.wrf	43.22
		482.sphinx3	53.26
		GEOMEAN	**47.48**

SPEC CPU2006/GHz performance of Kunminghu V2

Real Chips



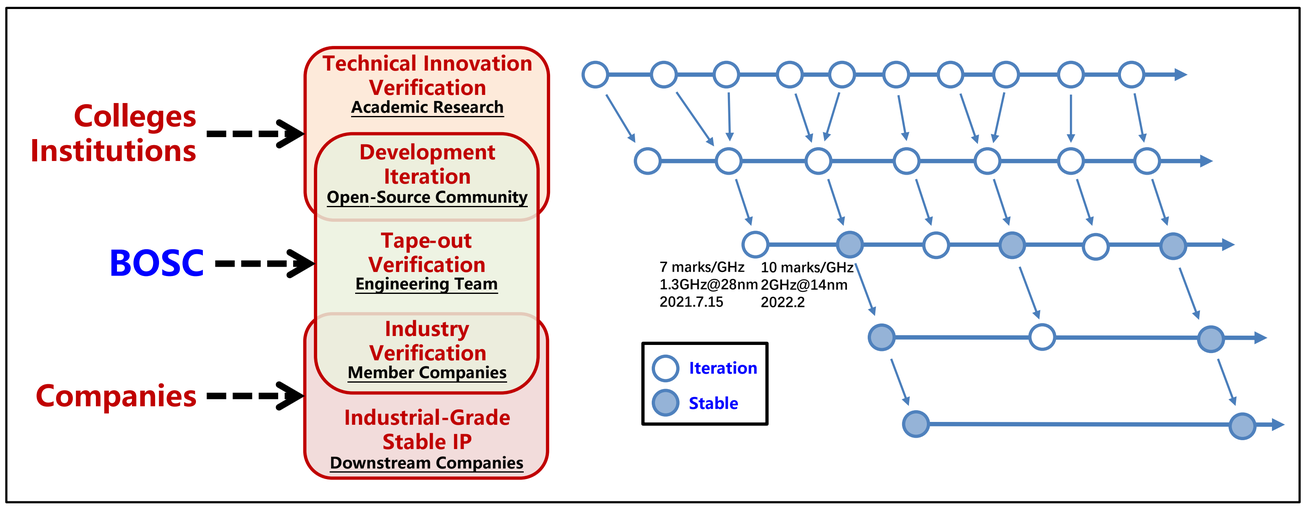
XS Gen1 Yanqihu
(1GHz@28nm)

XS Gen2 Nanhu
(2GHz@14nm)

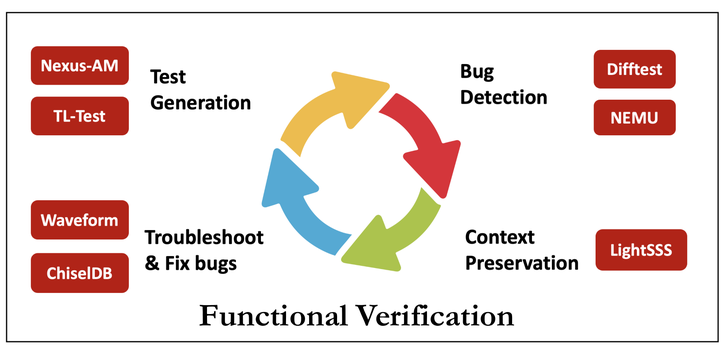
Ready to tape-out
XS Kunminghu V2 (3GHz@7nm)

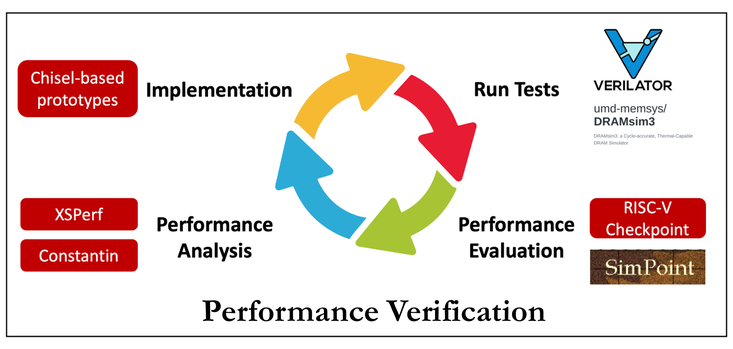
The Collaborative Mechanism Based on Open-Source Innovation

With high-level open-source hardware, we gather global innovative forces from various **colleges and institutions**, engaging in collaborative verification with **the industry**.



Agile Development Toolchain





Outlook

- With **three generations of optimization**, XiangShan Kunminghu V2 meets the needs from both academia and industry
- **Agile development toolchain** support rapid iteration
- **The new mechanism** brings academia and industry together

Welcome to Join Us !

XiangShan Source Code Repo: https://github.com/OpenXiangShan
Docs: https://docs.xiangshan.cc
Email: all@xiangshan.cc
Institute Website: https://bosc.ac.cn

Github Repository
WeChat Official Account