RIVeT-Co: Time-Predictable RISC-V based Vector Co-processor for High-Performance Computing

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Abstract

High-Performance Computing (HPC) is becoming increasingly important as the demand for more computational power grows across various domains like artificial intelligence, embedded systems, and medical research. The applications in these domains often involve complex simulations, large-scale data analysis, and advanced modeling, which require potent hardware and software to process data efficiently. Modern real-time embedded systems utilize various timing-aware scheduling strategies for the efficient execution of such high-performance applications. However, in the absence of a specified worst-case execution time (WCET), it is difficult to provide a predictable execution time for applications running on these systems. WCET is essential for real-time systems where timely responses to events are critical for correct system operation, especially in safety-critical applications like medical devices or automotive control systems. In this article, we propose a RISC-V-based vector co-processor that exhibits consistent and repeatable timing behavior, free from timing anomalies, thus enabling precise and efficient Worst-Case Execution Time (WCET) analysis. Unlike conventional high-performance vector processors that may suffer from execution-time variability due to speculation, caching, or data-dependent control flow, our design maintains predictability without sacrificing performance, making it suitable for real-time and safety-critical applications.

Introduction

The study of real-time computing has been a well-established research domain for many years. One prerequisite to confirm that a real-time system is operating correctly is time predictability. It has been observed in the state-of-the-art that the entire system can be drastically simplified using time-triggered architectures, or scheduling mechanisms in order to prevent undesired timing interactions. To provide the necessary timing predictability, [1] uses probabilistic real-time theory to take advantage of the new application timing constraints. To meet the demands of massively parallel processing workloads in terms of performance, [2] presented a timing predictable vector co-processor. However, these works do not focus on designing a processor or a co-processor tailored for better efficiency without harming the performance of data-parallel workloads in the *HPC* domain which is lacking in state-of-the-art. In this work, we propose a *RISC-V*-based time-predictable vector co-processor (*RIVeT-Co*). To ensure time-predictable execution, our *RIVeT-Co* design avoids traditional timing pitfalls by eliminating dynamic hardware behaviors such as caching, branch speculation, and out-of-order execution. All functional units are pipelined with fixed latencies, and instruction execution is governed by a centralized controller that dispatches operations deterministically based on the instruction type and vector length. These design choices result in a co-processor that is fully analyzable for WCET, fulfilling the requirements for timing predictability while still benefiting from vector parallelism. We demonstrate performance impact with standard vector benchmarks suite [3], which contains *HPCA* applications.

Our contributions are summarized as follows:

1. We present a 32-bit timing-predictable vector co-processor with five different functional units which is 100% compliant with RIC-V vector extension version-0.10.
2. We are considering a maximum Vector Length (VL) of 1024 bits.

Proposed Vector Co-processor Architecture

This section introduces the proposed *RIVeT-Co*, a 32-bit RISC-V-based in-order vector co-processor architecture which is time-predictable as shown in Fig. 2. with integer and fixed-point instructions of the RISC-V ISA. Vector processing capabilities are added to the instruction set by the V extension of RISC-V. It is integrated with the main scalar processor cv32e40x [4]. Table [**1**] shows experimental results of *HPC* applications of RiVEC Benchmark suite. It is a 4-stage in-order pipeline RISC-V core with RV32IMAC

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S. No.	Applications	Time Predictability (Expected No. of cycles)
1.	axpy	2,184
2.	spmv	9,000
3.	matmul	50,000

Table 1: *Time Predictability of High Performance Computing Applications of RiVEC Benchmark Suite*

instruction set. *RIVeT-Co* consists of a number of specialized functional units (VALU, VLSU, VMUL, VSLD, VIXU), each of which is in charge of carrying out a subset of the RISC-V vector instructions. Fig. 1 shows software workflow for application development on RIVeT-Co..

RIVeT-Co consists of the following functional units:

- VALU: Vector Arithmetic and Logical Unit.
- VLSU: Vector Load and Store Unit
- VMUL: Vector Multiplier Unit.
- VSLD: Vector Slide Unit.
- VIXU: Vector Indexing Unit.

CORE-V eXtension Interface (CV-X-IF)

Core-V eXtension Interface (CV-X-IF) [5] facilitates smooth co-processor support. Even without changing the CPU's decode unit, the CV-X-IF can actually improve the CPU with standardized or customized instructions for co-processor support. The first CPU with this interface is the cv32e40x [4].

Timing Predictability

To avoid thoroughly investigating every potential timing behavior for a safe WCET bound estimate, it is crucial to focus on both timing predictability and timing compositionality. We use timing predictable core SIC [6] approach to show that *RIVeT-Co* is free of timing anomalies in our vector processing. Initially, we establish the sequence of pipeline phases in eq.1, with subsequent pipeline stages signifying greater advancement:

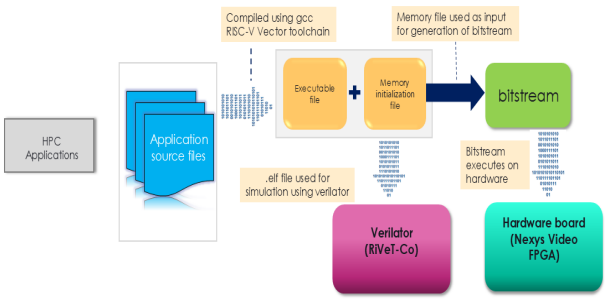

Figure 1: *Software Workflow for RIVeT-Co*

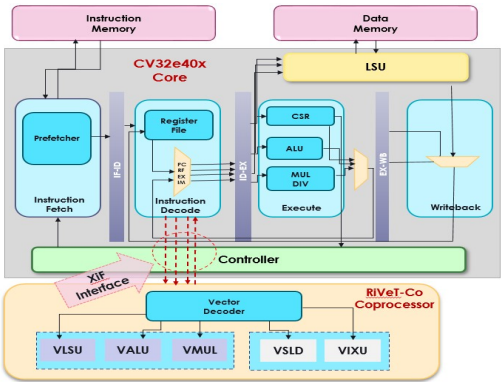

Figure 2: *Proposed Architecture of RIVeT-Co*

$$pre_{\mathcal{S}} IF_{\mathcal{S}} ID_{\mathcal{S}} EX_{\mathcal{S}} MEM \begin{matrix} \Sigma_{\mathcal{S}} \\ \leftarrow_{\mathcal{S}} \end{matrix} \begin{matrix} WB_{\mathcal{S}} post \\ ST \longleftarrow_{\mathcal{S}} \end{matrix} \quad (1)$$

Discussion

The timing predictability of current processor designs is hindered by performance-enhancing features. Consequently, processors which are optimized for high computational throughput outperform those designed for time-sensitive systems. However, more potent systems are needed to manage complicated parallel workloads due to the ever-increasing demands of high-performance and real-time applications. In this work, we have presented a *RIVeT-Co*, a 32-bit RISC-V vector extension based on massively parallel processing that is scalable, efficient, and timing-predictable. By integrating vector architecture with the cv32e40x processor as the primary core, we have shown that there are no timing anomalies in the combined processing system, allowing for compositional timing analysis.

References

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