RIVeT-Co: Time-Predictable RISC-V based Vector Co-processor for High-Performance Computing

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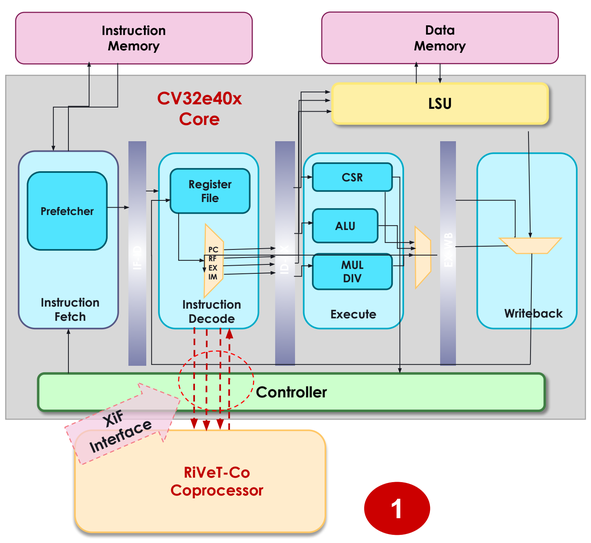
Motivation

- Modern vector processors deliver impressive performance but are often plagued by timing unpredictability due to dynamic behaviors like speculative execution, caching, and variable memory latency.
- This unpredictability hinders their deployment in real-time and safety-critical systems, where Worst-Case Execution Time (WCET) bounds must be known to guarantee correct system behavior.
- **Time-Predictable RISC-V-based vector coprocessor** that delivers consistent, repeatable timing behavior suitable for static WCET analysis—bridging the divide between high-performance computing and real-time systems.

Introduction

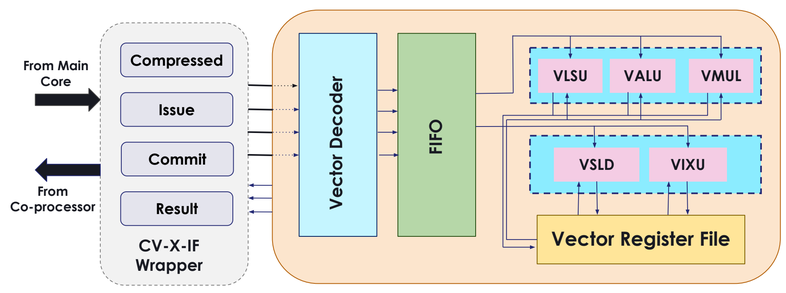
- RIVeT-Co, a 32-bit RISC-V-based in-order vector coprocessor architecture which is time-predictable integrated with the main scalar processor cv32e40x using cv-x-if interface protocol.
- RIVeT-Co consists of a number of specialized functional units (VALU, VLSU, VMUL, VSLD, VIXU with dual configuration, each of which is incharge of carrying out a subset of the RISC-V vector instructions.
- All functional units are pipelined with fixed latencies, and instruction execution is governed by a centralized controller that dispatches operations deterministically based on the instruction type and vector length.

Block Diagram



1

Overall Architecture of a system



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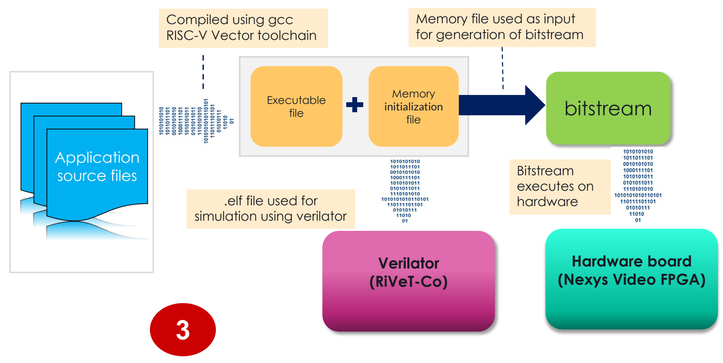
Microarchitecture of RIVeT-Co

HPC Applications



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Simulation Workflow

Results

Experimented results of standard Benchmarks of high performance computing applications from **RiVEC Benchmark Suite.**

These are the following applications:

1. **axpy**: $y[i] = a * x[i] + y[i]$
2. **spmv**: $y[i] = \sum A[i][j] \cdot x[j]$, for all $j \in$ nonzeros of $A[i,:]$
3. **matmul**: $C[i][j] = \sum_{k=0}^{n-1} A[i][k] \cdot B[k][j]$

S.No.	Applications	Time Predictability (Expected No. of cycle)
1.	axpy	2,148
2.	spmv	9,000
3.	matmul	50,000

Conclusion

- We proposed time-predictable RIVeT-Co, a 32-bit RISC-V-based vector co-processor designed to deliver both high computational throughput and timing predictability, addressing a critical need in real-time high-performance systems.
- By leveraging a scalable and parallel vector architecture tightly integrated with the cv32e40x core, RIVeT-Co eliminates common sources of timing anomalies—such as speculative execution, dynamic caching, and variable-latency pipelines.

Future Work

- Future work will focus on enhancing both the architectural and software aspects of RIVeT-Co to broaden its applicability and efficiency.
- On the software side, efforts will be directed toward developing compiler-level optimizations that can fully exploit RIVeT-Co's predictable parallelism.

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