Enabling Reconfigurable High-Throughput RISC-V Systems through Barrel Processing.

Institut für Technische Informatik

Novel Computing Technologies

Dr. -Ing Riadh Ben Abdelhamid and Prof. Dr.-Ing. Dirk Koch

UNIVERSITÄT HEIDELBERG ZUKUNFT SEIT 1386

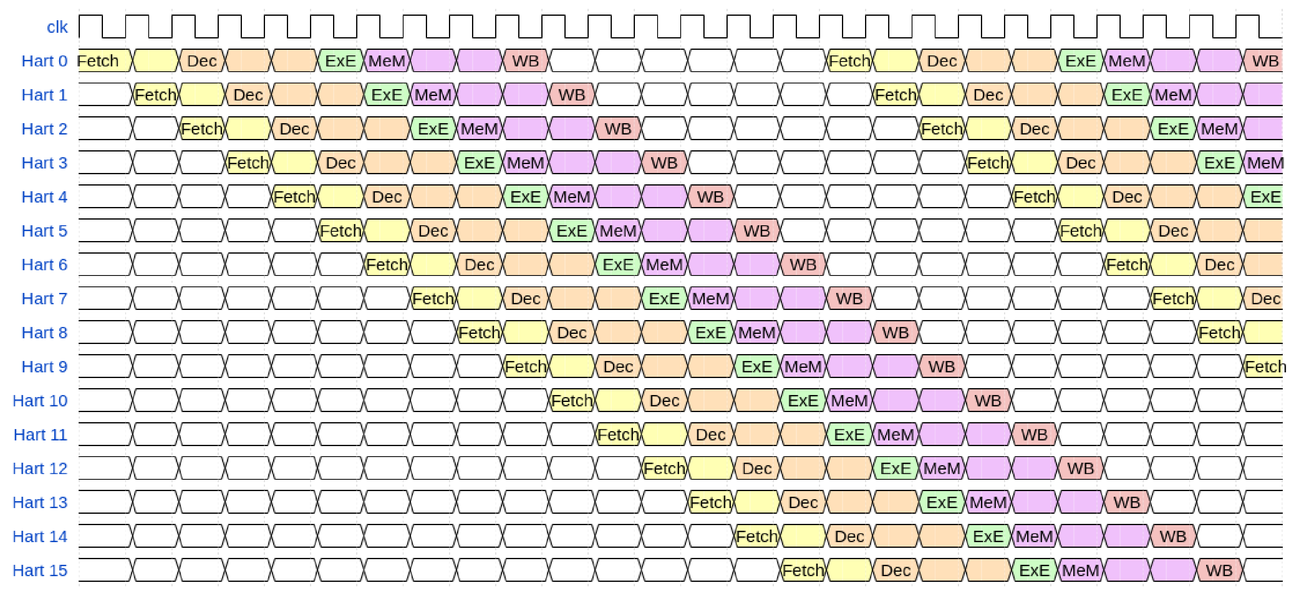
BRISKI (Barrel RISC-V for Kilo-core Implementations)

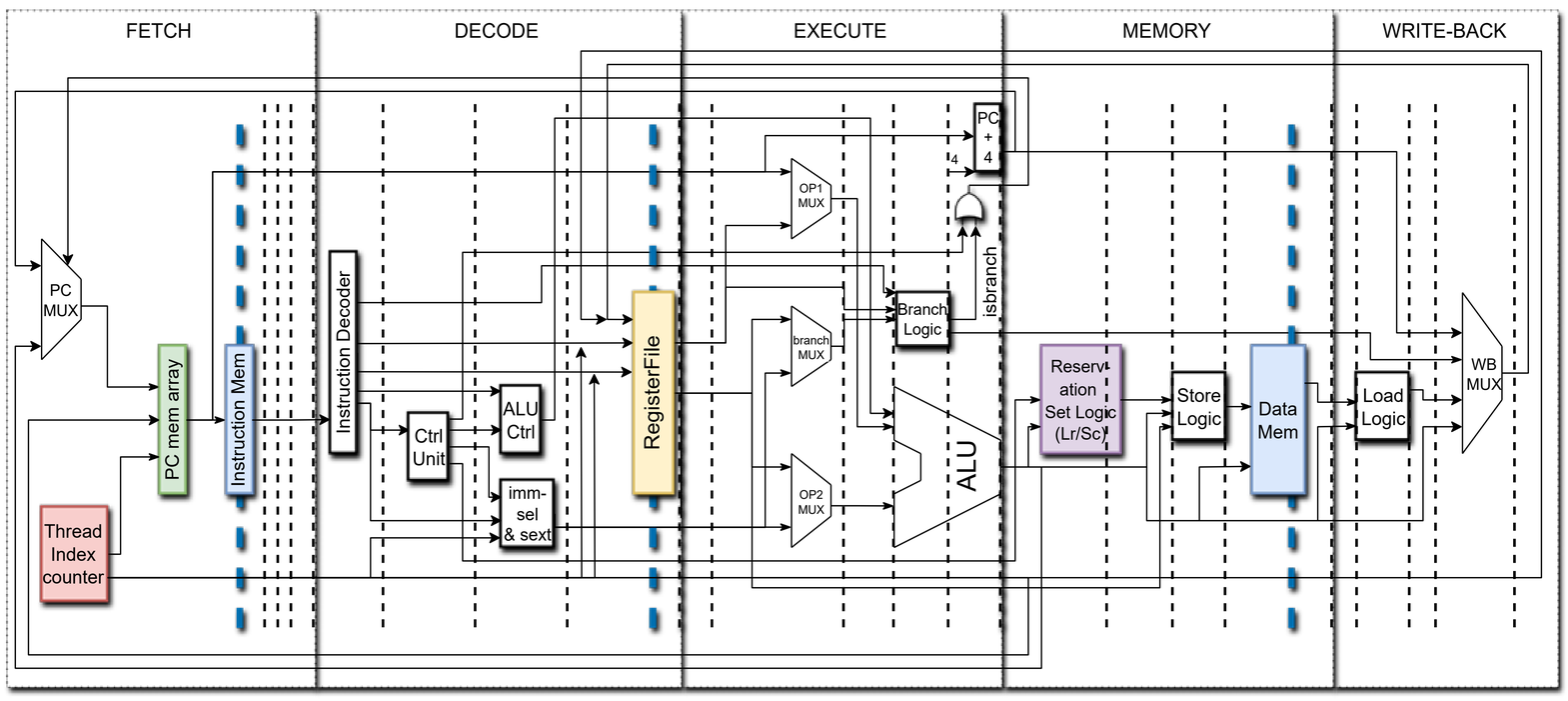
- A highly-optimized, fast and compact RISC-V Barrel Processor core:
  - **Area : 400 ~ 800 LUTs**
  - **Speed :** Up to **@ 737 MHz (BRAM speed limit on VU9P (speed grade 2))**
  - **CPI =1**
- **ISA : Full RV32I** user-mode, **CSRRS** and **Zalrsc** (Atomic instructions subset)
- **Memory:** 4 KB/core shared I-RAM and D-RAM (+ multiple cores can share URAM)
- **Publicly available** under:

https://github.com/riadhbenabdelhamid/BRISKI

Barrel Processing

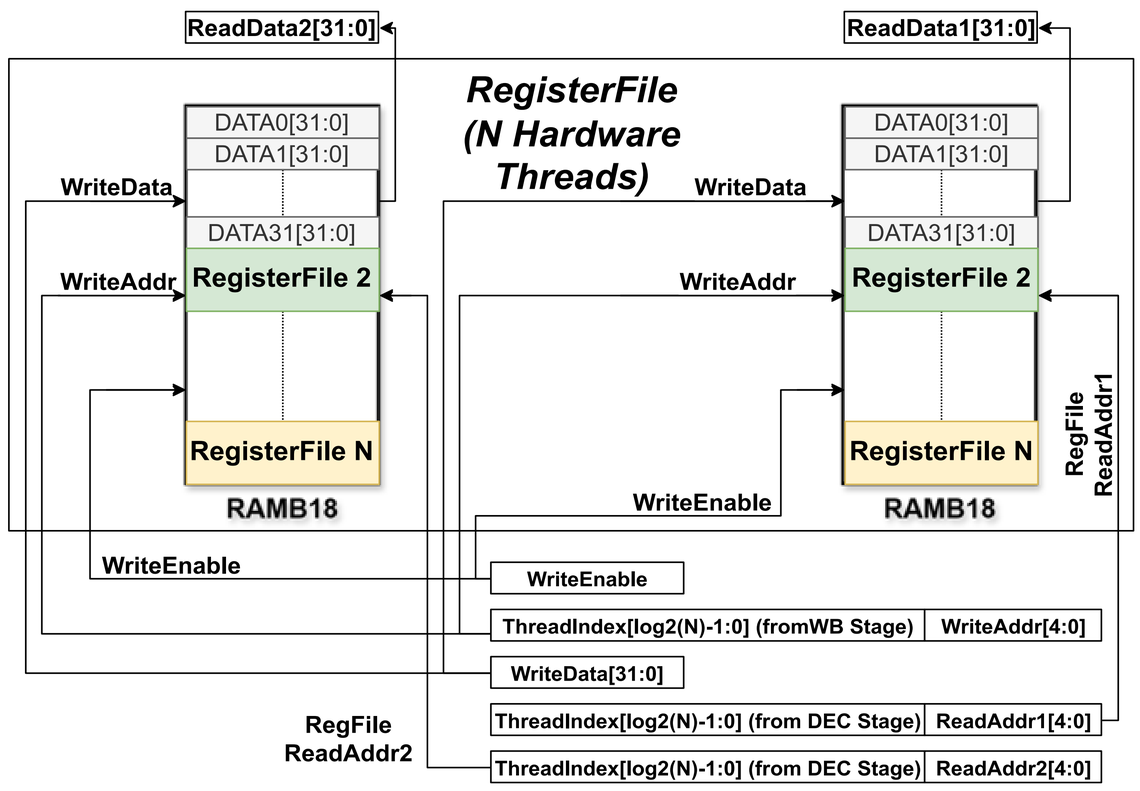
- **Interleaved** Thread Execution (Round Robin)
- When threads are restarted **all hazards are resolved**

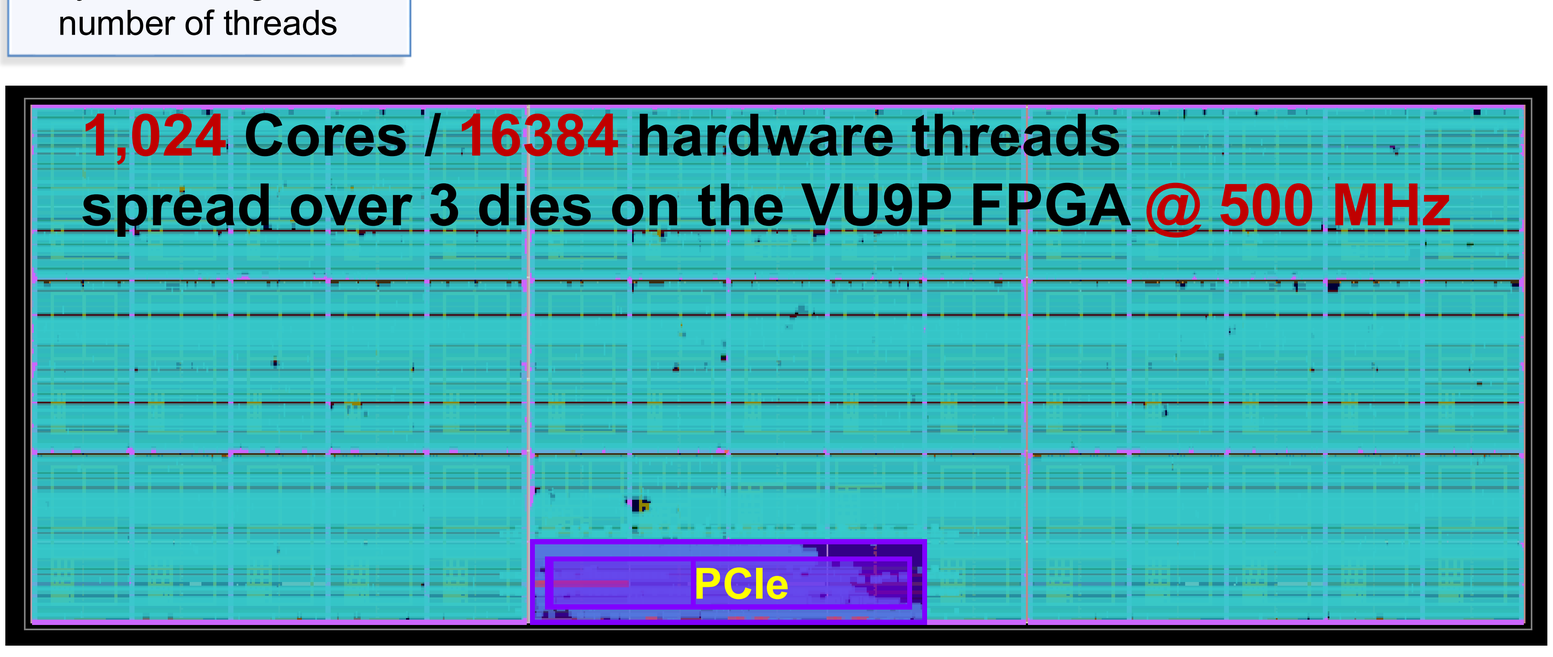




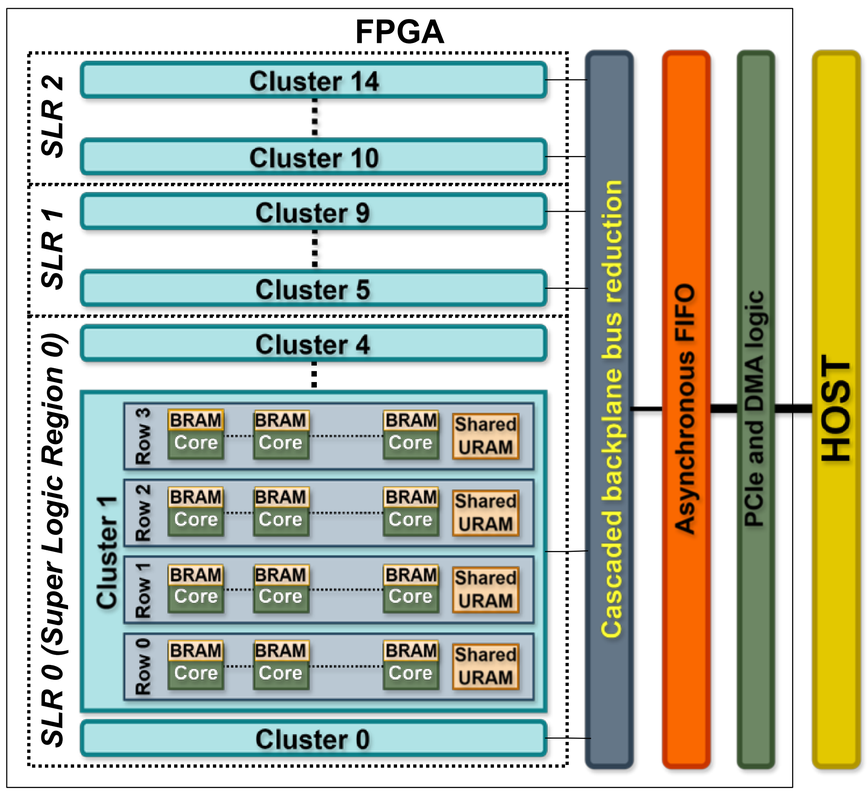
BRISKI's reconfigurable parameters

- Threads (4 to 16).
- Pipeline depth (4 to 16 physical stages)
- Some ALU operations can be implemented through DSPs.
- Barrel Shifter optimization (Speed target vs Area target with unified implementation).
- Hardware barriers to avoid slow LR/SC sync with large number of threads

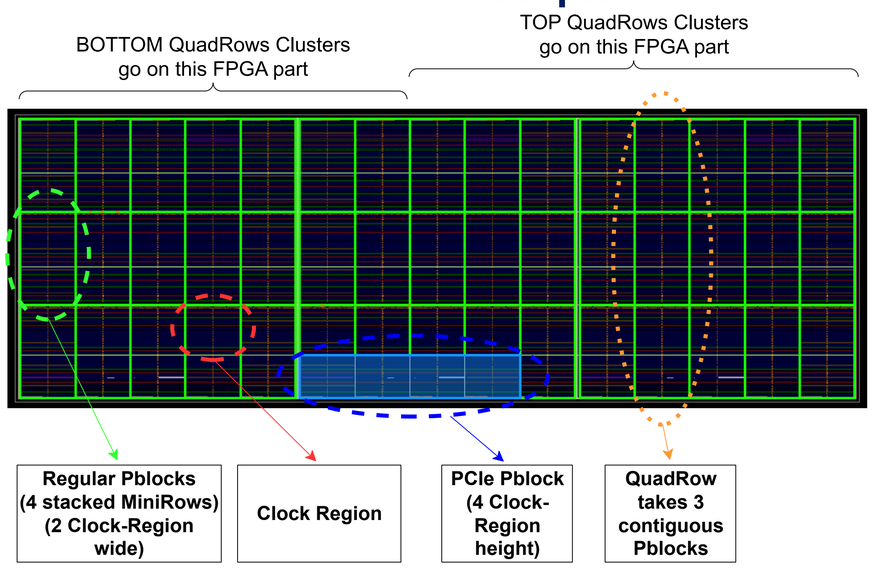




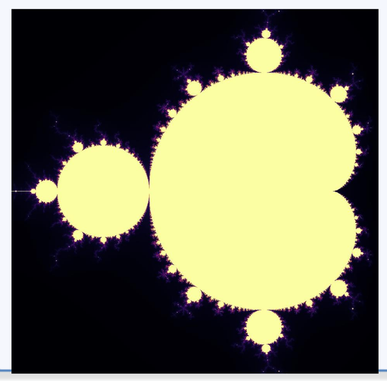
SPARKLE Architecture



SPARKLE floorplan



Mandelbrot Set as computed on SPARKLE: 1,024 by 1,024 resolution (64 pixels per thread).



Example Applications

- **Fractals (Mandelbrot, Julia Sets, etc.)**
- Massively parallel DNA sequence alignment
- Monte Carlo simulations

Highest RISC-V Instruction throughput on any FPGA Implementation

	OoO [4], 2019	in-order [5], 2016	**Barrel** [11], 2025
FPGA	XC7Z020	VU9P	VU9P
LUT	∼15k	**320**	646
BRAM	6	0.5-1**	1
ISA	RV32IM	RV32I+lr/sc-bshift	RV32I+lr/sc+csrrs
F_{MAX}	95.3 MHz	375 MHz	**737 MHz**
MIPS/LUT	0.012	0.73 [5]	**1.14**

Update of SPARKLE : Manycore design based on 1,024 BRISKI cores (16,384 hardware threads) @ 500 MHz

Baseline version:

- **< 800K** LUTs on **VU9P**
- **100% DSPs usable for accelerators**
- **@400 MHz → 400 GIPS**
- High Compute Density: **~0.5 MIPS/LUT**
- **Includes a PCIe host interface.**

Enhanced version:

- **630K-800K** LUTs on **VU9P**
- **1,024 DSPs may be used for partial ALU implementation.**
- **@500 MHz → 500 GIPS**
- High Compute Density: **~0.81 MIPS/LUT**
- **Includes a PCIe host interface. Backplane bus @500MHz**