REPTILES: Repeated Tiles of Sargantana, a RISC-V multicore based on OpenPiton

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Abstract

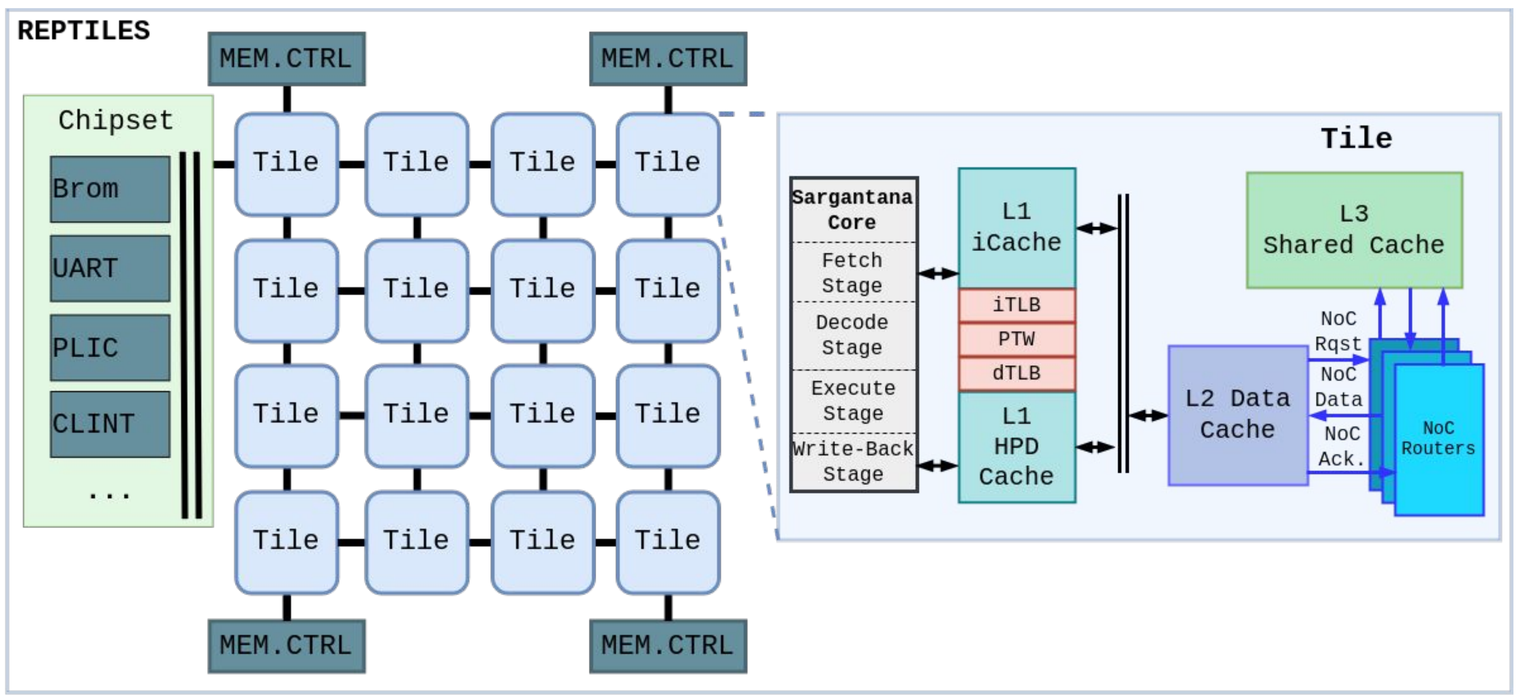
Chip industry continues advancing and expanding modern computing systems, resulting in **more complex multi-core processors**. Conversely, **academic projects** face scalability challenges due to **limited resources and infrastructure**. The **community needs open-source frameworks** that enable innovation and knowledge sharing.

This work presents **REPTILES, REP**eated **TILE**s of Sargantana**,** an **open-source RISC-V multicore framework** based on Sargantana and OpenPiton. We aim to provide an accessible HPC framework where researchers can develop, experiment with, and optimize HPC applications. Additionally, we show the new features incorporated in OpenPiton and Sargantana designs to improve the performance of HPC applications. Finally, we demonstrate that REPTILES present a suitable scalability achieving a speedup of 3.1× on average with 4 cores.

Contributions

REPTILES is based on the open-source designs: **OpenPiton and Sargantana**

- **OpenPiton** is a multi-core framework which consists of a chipset and one or more tiles. It operates in different architectures, such as SPARC v9, x86 and RISC-V.



- **Sargantana** is a Linux-capable 64-bit RISC-V processor that implements the RV64GV ISA.

OpenPiton Improvements

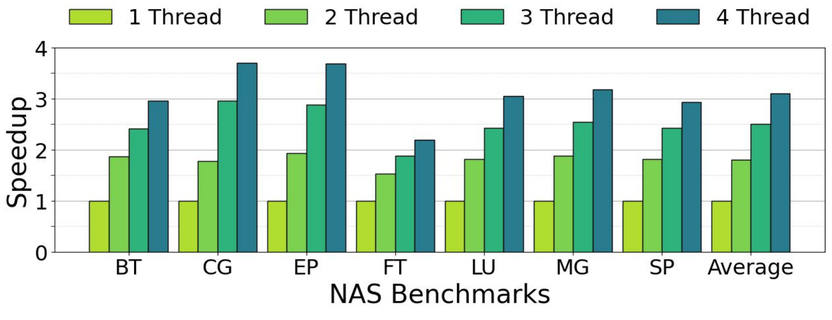
- Parametric **NoC width**: 64, 128, 256, 512 and 704 bits.
- Parametric **cache block sizes**: 16, 32, and 64 bytes.
- Parametric **number of MSHRs** in all cache levels: from 2 up to 64.
- Parametric **cache sizes and associativities.**
- **Support for parallel SRAM access** in the L2 and L3 caches.
- **Enhanced design** with the connection of Sargantana to the **High-Performance Data Cache** (HPDCache).

Sargantana Improvements

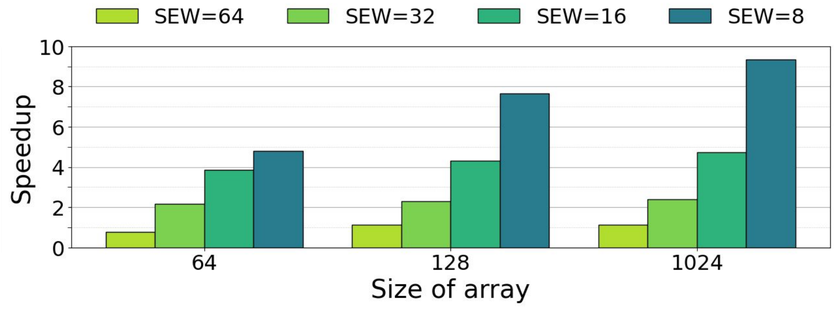
- **Upgraded RISC-V Vector Extension** (RVV) from version 0.7 to **1.0**, configurable from 128 to 512 bits (in this poster, 128).
- **Added support for most of the RVV specifications**, except for the LMUL>1 setting and vector FP instructions.
- **Added RISC-V extensions Sdext** (for debugging support) and **Sscofpmf** (to enable reading core performance counters in Linux via perf).

Results

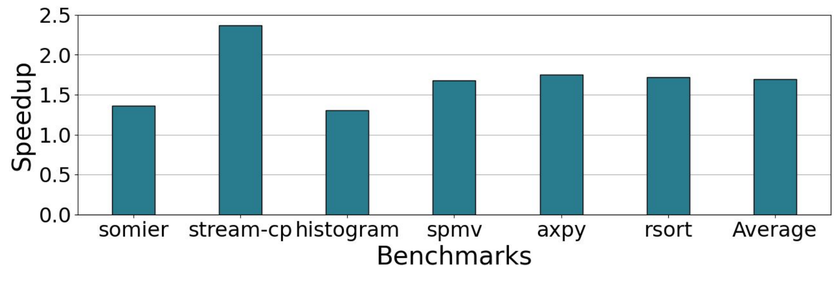
- Increasing number of threads demonstrates **suitable scalability,** 3.1x on average.
- CG and EP achieves 3.6x and 3.1x, respectively



- The vectorization of a matrix addition shows up to 9.3x speedup when using a Standard Element Width (SEW) of 8 bits and Vector Length (VLEN) of 128 bits.



- The OpenPiton HPC improvements provide 1.7x speedup on selected benchmarks.



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Open-Source Code