Towards an Industrial-Grade Open-Source Floating-Point Unit for RISC-V Vector Processors

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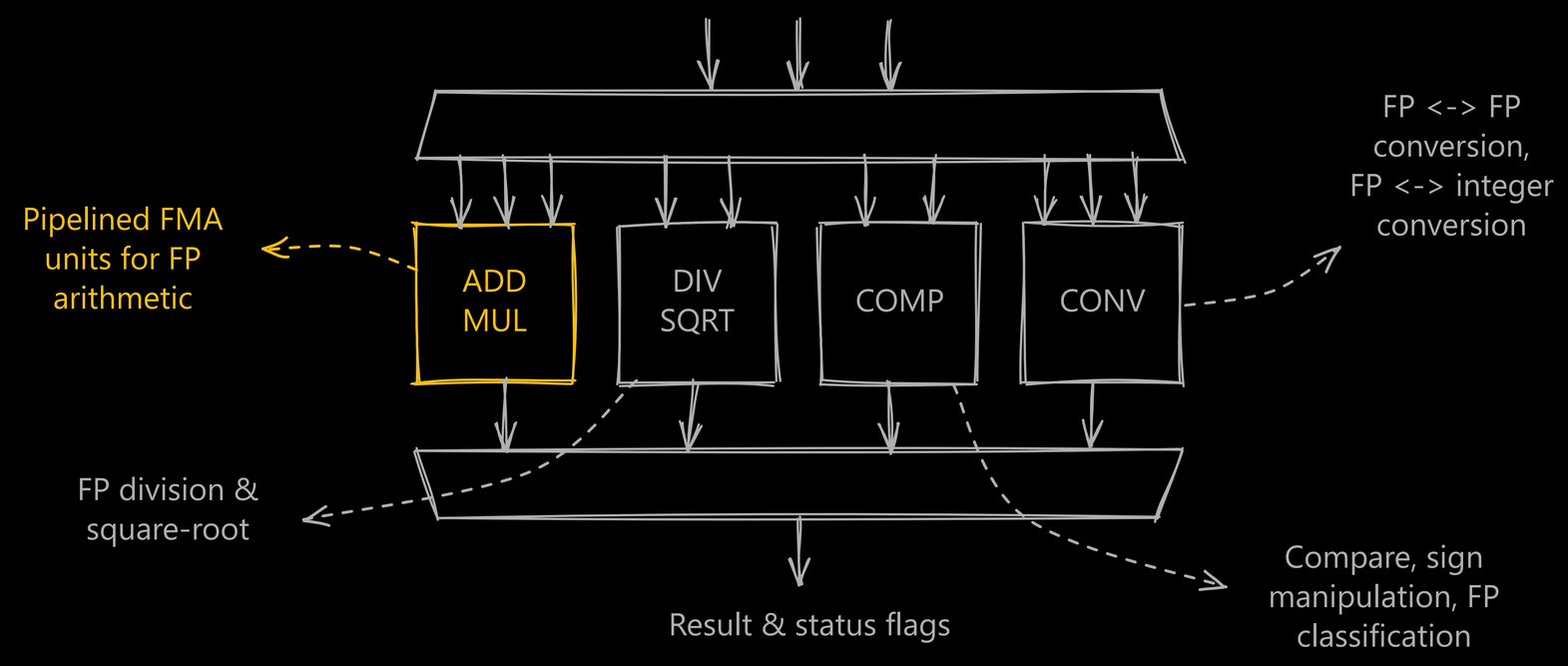
Parametric floating-point unit with support for standard RISC-V formats and operations as well as transprecision formats
Formerly known as FPnew, developed at ETH Zürich [1]



Contributions for Improved Vector Support

- Symmetric Widening Add

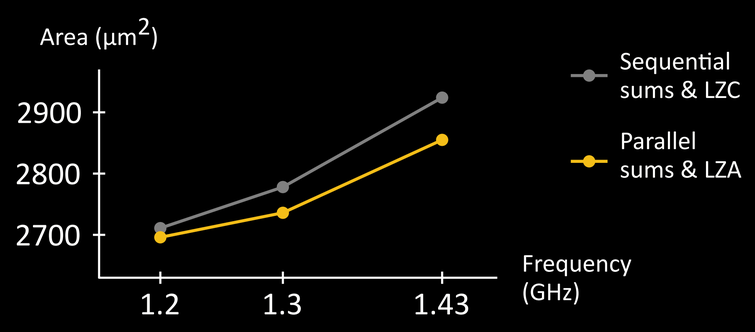
  Added *symmetric* widening add (same width operands) in addition to *asymmetric* add (one narrow, one wide operand) for V extension support

- FMA Datapath Improvements

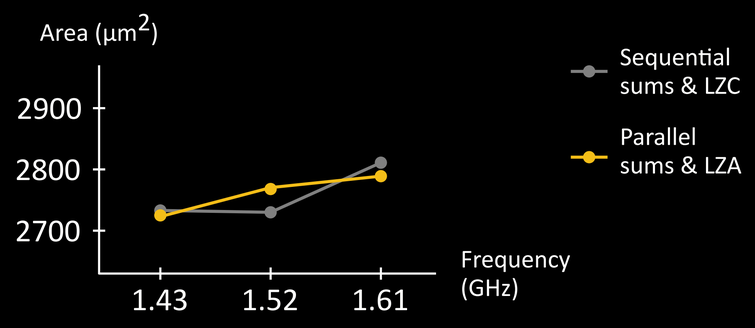
  Parallel positive & negative sums to avoid two sequential adder carry chains

  Leading Zero Anticipator (LZA) to calculate shift amount in parallel with sums

Area vs Timing Improvement w/o Retiming

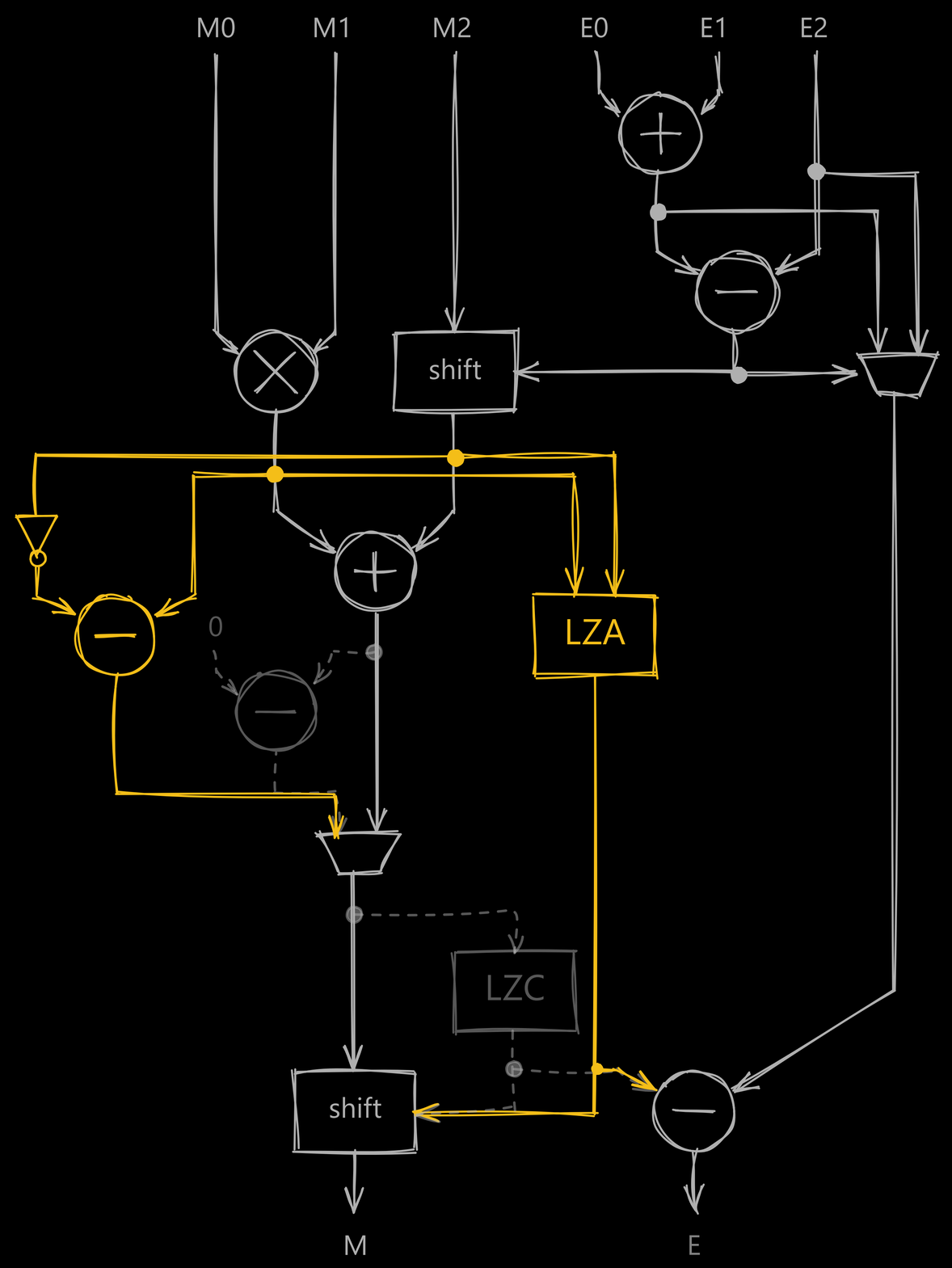


Area vs Timing Improvement with Retiming



- Extend RISC-V DV with V extension

  Random instruction generator RISC-V DV (maintained by CHIPS Alliance) extended with V extension support



† OpenHW Group CVFPU
github.com/openhwgroup/cvfpu

[1] Mach, Stefan, et al. "FPnew: An open-source multiformat floating-point unit architecture for energy-proportional transprecision computing." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems 29.4 (2020)*: 774-787.

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