#### Politecnico di Torino A Deep Dive into Integration Methodologies in RISC-V

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Alessandra Dolmeta<sup>1</sup>, Valeria Piscopo<sup>1</sup>, Maurizio Martina<sup>1</sup>, Guido Masera<sup>1</sup>

**1** Politecnico di Torino, DET - Dipartimento di Elettronica e Telecomunicazioni , Turin, Italy

## Introduction

- In embedded systems design, the growing computational demands have driven the integration of specialized accelerators. The integration methodology can significantly affect their performance:
  - Loosely coupled accelerators are generally memory-mapped and operate independently, interfacing with the CPU via a system bus.
  - Tightly coupled accelerators are integrated within the CPU microarchitecture and directly access internal registers.
     Coprocessors differ by utilizing external register files.

### • **Coprocessor** (Figure 4):

Hybrid between loosely and tightly approaches: leverages CV-X-IF but accelerates the complete Keccak-f permutation.

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- Three R-type custom instructions to store/load the state into the dedicated Keccak register file and to start the permutation. Instructions called via inline assembly.
- Not fully RISC-V compliant.
- RISC-V's open-source ecosystem has further advanced accelerator research. The Core-V eXtension InterFace (**CV-X-IF**) [1] facilitates tightly coupled accelerator integration without modifying the CPU toolchain and pipeline.
- The analysis of different integration methodologies is applied to Keccak, a pivotal hashing standard in Post-Quantum Cryptography (PQC): we present KRONOS, a Keccak RISC-V Optimized eNgine for haShing.



CV-X-IF

The CV-X-IF interface introduces a dispatcher that enables the integration of custom instructions without modifying the existing core components, preserving the original decoder, ALU, and RF (*Figure 1*).
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• We take **SHA3-384** function as a case of study to test the three versions of KRONOS. SHA3-384 is part of the SHA-3 family, which is based on the **Keccak** cryptographic permutation: evaluating SHA3-384 directly tests the performance of KRONOS.

Results

• *Table 1* illustrates the **cycle counts** for executing the SHA3-384 function on X-HEEP platform using the three different methods, and their relative speed-ups and throughput. The -O2 flag is used for reference and accelerated simulations.



# Integration methodologies

Three versions of KRONOS are presented. They are integrated into X-HEEP [2], a RISC-V based microcontroller, using the CV32E40PX core [3].



Figure 2. Loosely coupled approach.

- Loosely coupled (Figure 2):
   Memory-mapped component, accelerating the complete Keccak-f permutation.
  - Fifty 32-bit registers to store the state.
  - KRONOS called by a dedicated driver.

Table 1. Cycle counts – SHA3-384.

Method	Ref.	Accel.	Speed-up	Thr.
			factor	[Mb/s]
Loosely		4,169	$13.56 \times$	4.61
Tightly	56,529	$31,\!527$	1.79  imes	0.61
Coproc		7,553	7.48  imes	2.54

• *Table 2* presents a comparison of the FPGA **area** results for the three versions, implemented on the Zynq UltraScale+ ZCU104 board (xczu7ev-ffvc1156-2-e). The synthesis and implementation are performed using Xilinx Vivado, with a global clock of 50 MHz.

#### Table 2. Resource utilization (ZCU104, 50 MHz).

Method	LUT	Registers	Thr./Area
			$[kb/(s\cdot LUTs)]$
Loosely			
♦ KRONOS	4,915	3,252	
<ul> <li>Controller</li> </ul>	7	35	0.937
<ul> <li>Keccak</li> </ul>	4,908	1,617	
<ul> <li>Register File</li> </ul>	0	1,600	
Tightly			
♦ KRONOS	569	139	
<ul> <li>Controller</li> </ul>	569	102	1.070
○ rol_32	0	32	
Coproc			
♦ KRONOS	6,591	3,372	
<ul> <li>Controller</li> </ul>	1,181	125	0.386
<ul> <li>Keccak</li> </ul>	5,409	1,615	
<ul> <li>Register File</li> </ul>	0	1,600	



Tightly coupled (Figure 3):

 Leverages the CV-X-IF.
 RISC-V-compliant custom instruction rol\_32, accelerating the bitwise rotation operation. Instruction called through inline assembly.

 No additional register file

is used.

Figure 3. Tightly coupled approach.

• The optimal trade-off between area and throughput is provided by the tightly coupled version. The absence of a dedicated Keccak register file results in a substantially more compact solution when compared to the other integration methodologies.

