TECHNISCHE UNIVERSITÄT DRESDEN

ComNets
Deutsche Telekom Chair of Communication Networks

Faculty of Electrical and Computer Engineering, Deutsche Telekom Chair of Communication Networks

Towards a Base-Station-on-Chip: RISC-V Hardware Acceleration for wireless communication.

5G Lab GERMANY

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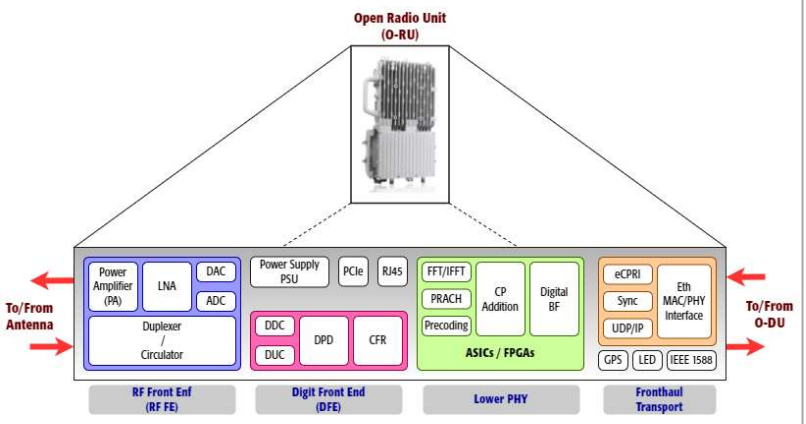
Overview

- Implementation of LOW Physical layer on vector DSP.
- Main kernels:
- Channel estimation $H = YX^{-1}$

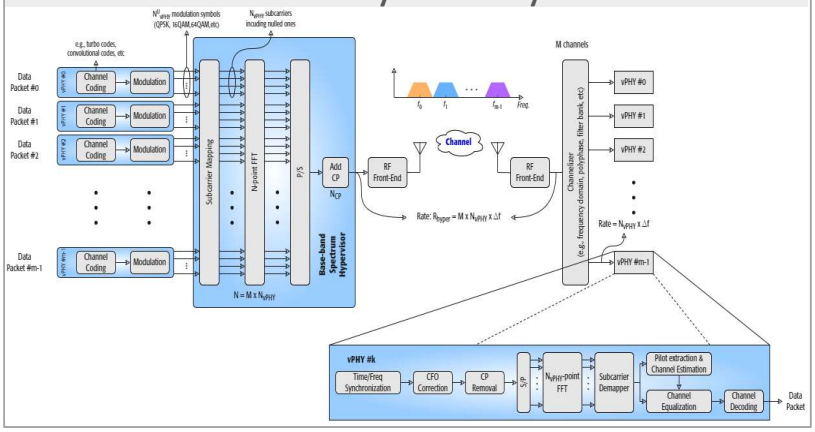
1. Channel estimation LSE $H = Yx^H(xx^H)^{-1}$
2. Channel estimation MMSE $H = x^H T^H(xTRx^H + \sigma^2 I)^{-1}Y$
3. Massive MIMO
4. Beamforming W = $H^H(HH\hat{}H)\hat{} - 1$

- Integration of those kernels onto a single chip to meet throughput and latency requirements.
- Leveraging the vectorization capabilities of the RISC-V vector DSP to execute matrix multiplication and inversion concurrently across parallel lanes.

Base station on Chip



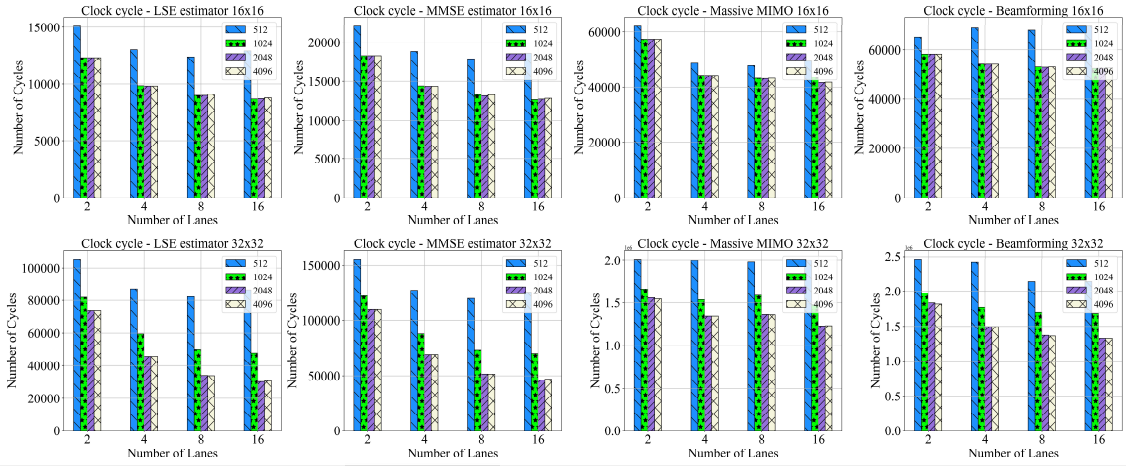
LOW Physical Layer



Future research directions

- Implementation of each wireless communication kernel in SystemVerilog
- Design and integration of tailored instructions to integrate custom hardware into the RISC-V Ara core
- Implementation of deep learning-based channel estimation.

Results



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