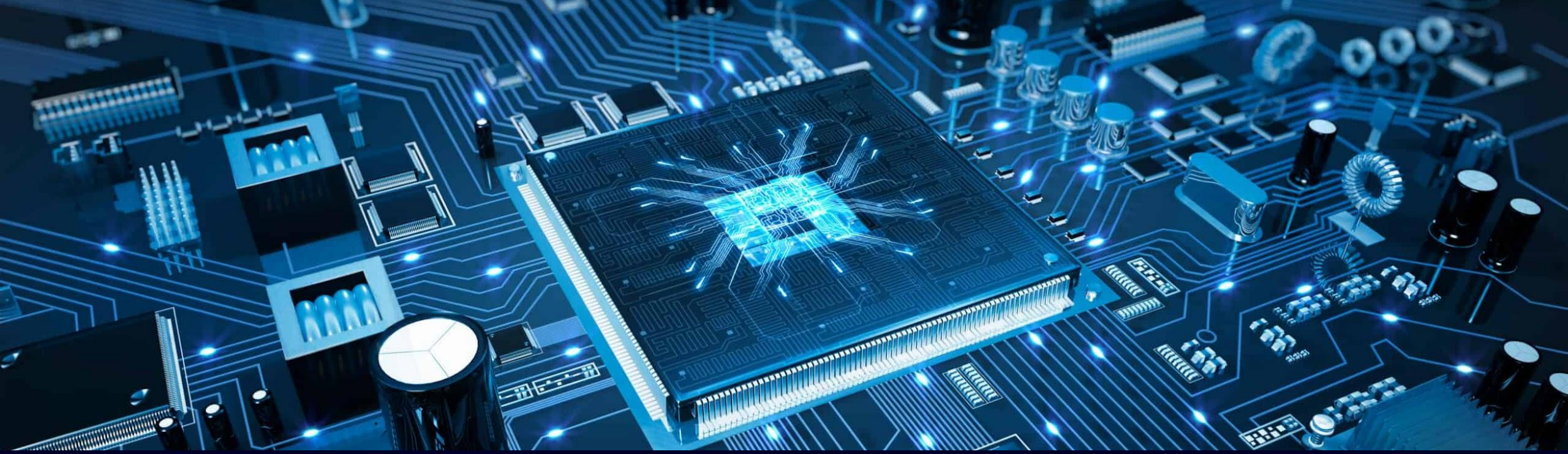


Enhancing your RISC-V SoC debug & optimization with embedded functional monitors

Mat O’Donnell, Software Architect Lead

Tessent Embedded Analytics, Siemens EDA

SIEMENS

Agenda

Functional Monitoring – what and why?

Mitigating issues for high bandwidth

Actionable insights – Customer Use Cases

Continuous in life monitoring

Summary

Functional monitoring – why?

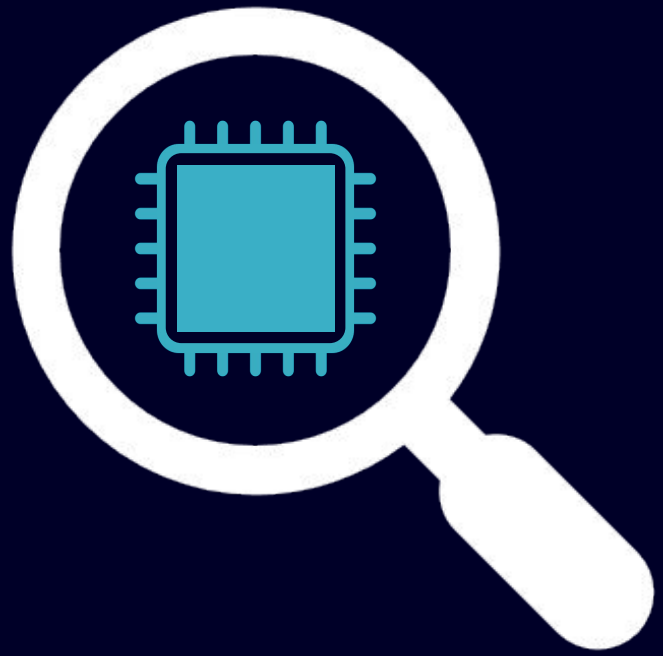
The effort required to validate, debug, and optimize SoCs continues to escalate

Need better ways to observe if SoCs behave and perform as intended

Reduces SoC debug effort prior to launch

Simplifies system performance optimization before and after launch

Enables in-life system health monitoring



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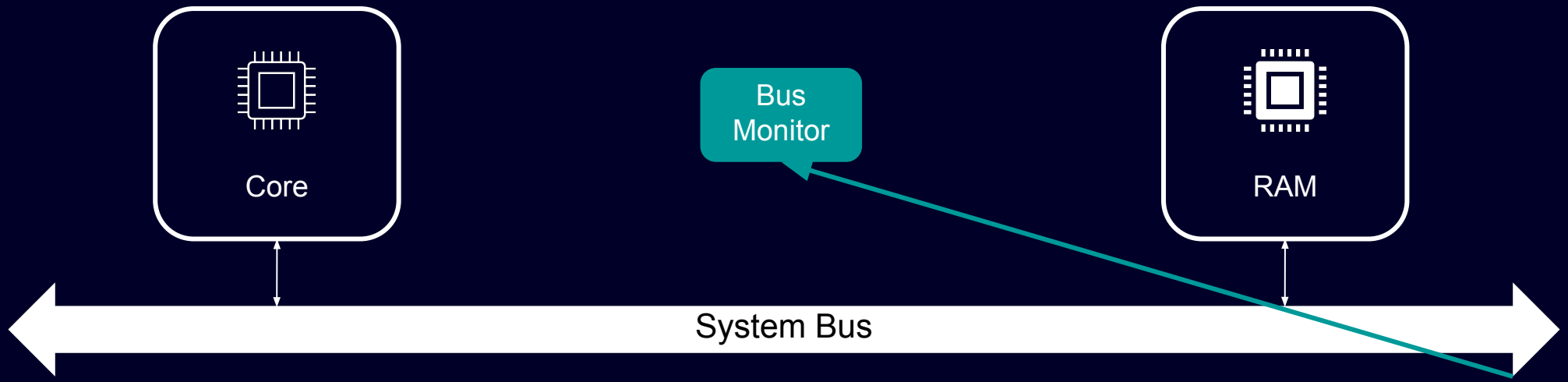
Functional monitoring – what?

Observing non-intrusively if your SoC behaves as it was designed



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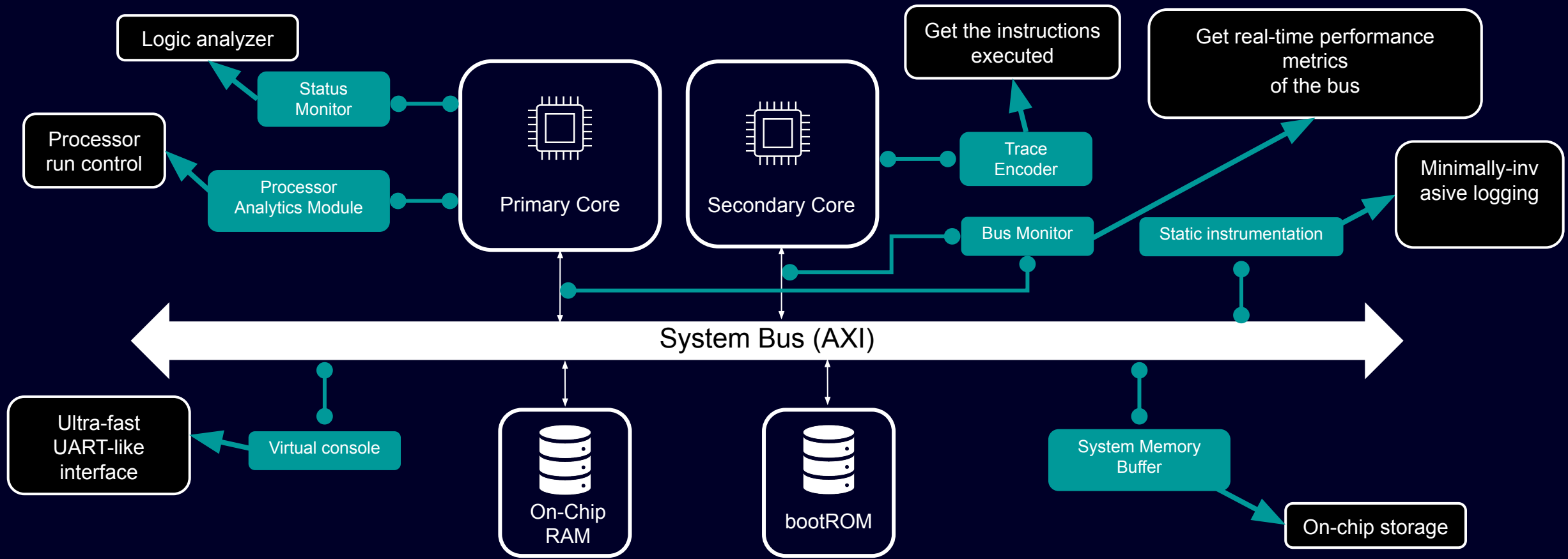
System-wide functional monitoring

Full system-level debug and functional monitoring provide additional insights



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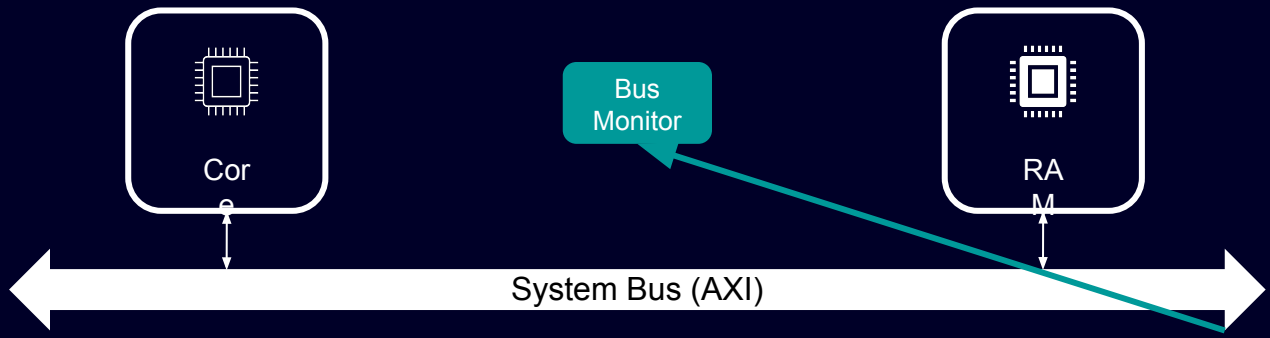
Mitigating issues for high bandwidth

- **Smart Filtering**
- Smart Logging
- Counters
- Cross-triggering

```
# configure filter for writes between two addresses
filter = hsdk.BusMonitor.Interface.Filter()
filter.address(0x60000000, 0x60054600, "inclusive")
filter.types("write")
```



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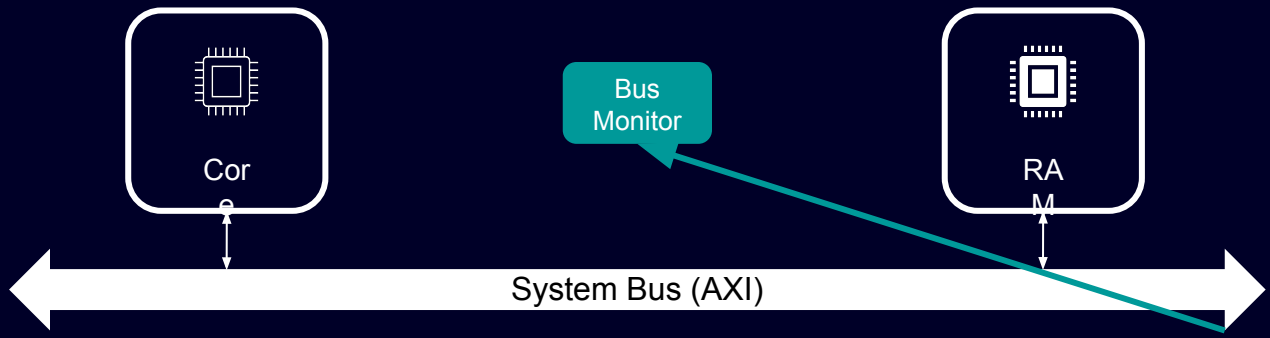
Mitigating issues for high bandwidth

- Smart Filtering
- **Smart Logging**
- Counters
- Cross-triggering

```
# configure filter
filter = hsdk.BusMonitor.Interface.Filter()
filter.types("write")

# trace any transactions that match the filter
trace = interface.trace(filter, "write_address")
```



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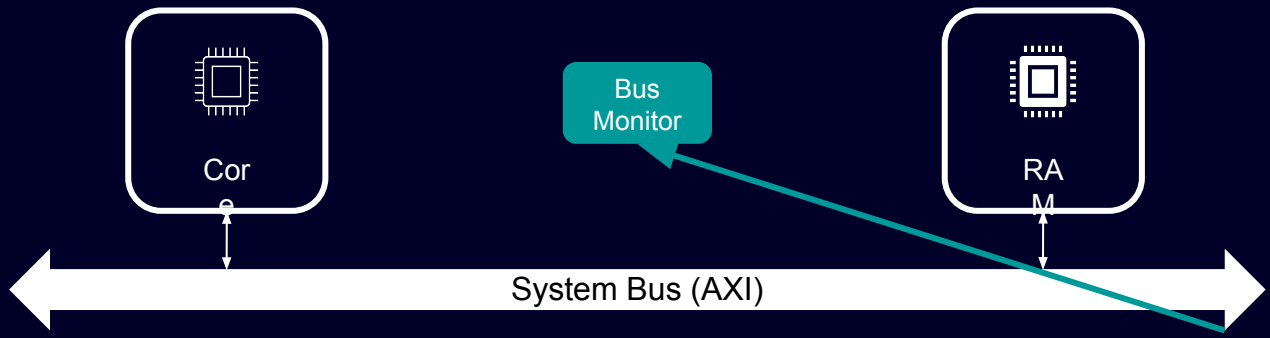
Mitigating issues for high bandwidth

- Smart Filtering
- Smart Logging
- **Counters**
- Cross-triggering

```
# configure filter
filter = hsdk.BusMonitor.Interface.Filter()
filter.address(0x60000000, 0x61000000, "inclusive")

# count the number of busy cycles
count = interface.count("busy_cycles", "count", filter)
```



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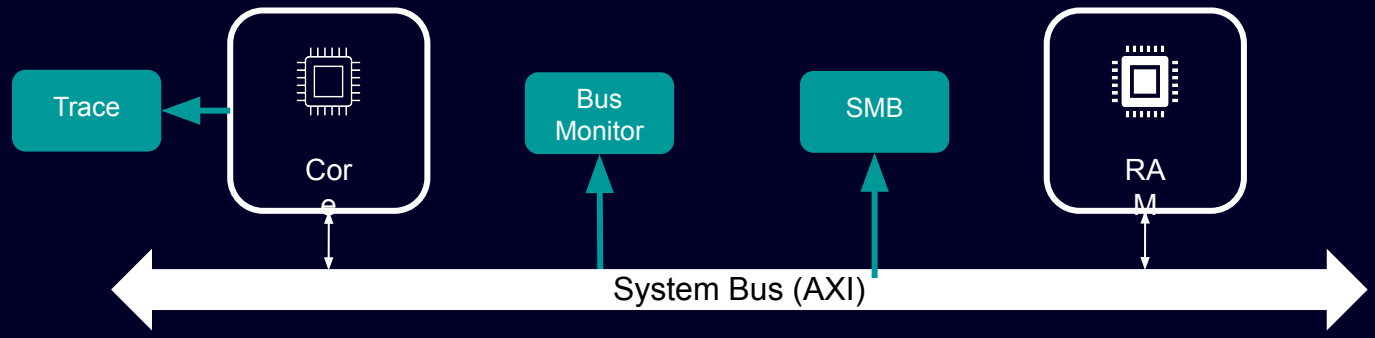
Mitigating issues for high bandwidth

- Smart Filtering
- Smart Logging
- Counters
- **Cross-triggering**

```
# configure filter
filter = hsdk.BusMonitor.Interface.Filter()
filter.address(0x60000000, 0x60000004, "inclusive")
filter.type("write")

# fire an event when the filter matches
event = hsdk.BusMonitor.Event()
bus_monitor.event(filter, event)

# configure SMB as a circular buffer
smb = hsdk.SMB("to")
smb.output_on(event)
```



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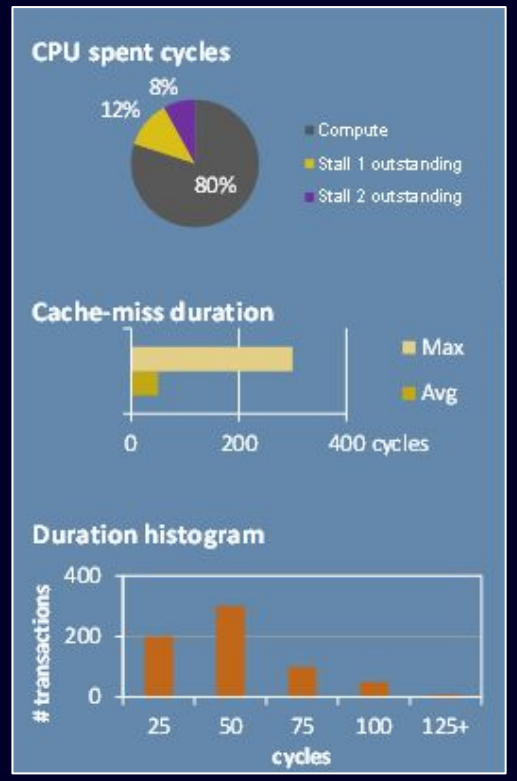
Monitoring for performance improvements

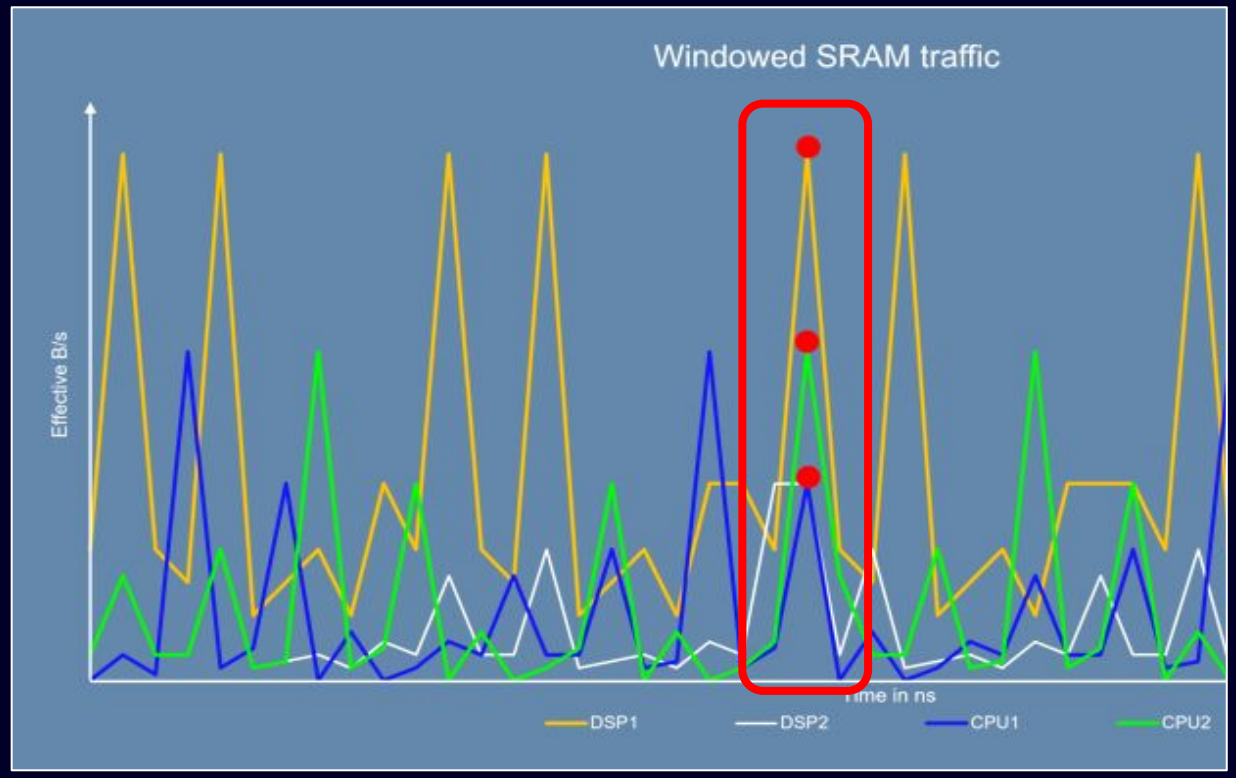
picocom
Empowering Wireless

CPU performance loss



Identified excessive max cache miss duration, which impacted overall performance

Memory bandwidth degradation



All cores try to access memory with high bandwidth simultaneously

Details: How Picocom optimizes 5G SoCs and networks with Tessent

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Functional monitoring for actionable insights

soc_noc_rt0=>{0x3E02_0000 to 0x3E02_8000 }

1. Address: 0x00000428 Name: region55_subregion1_cnr_if_snoc_uaxia_m_ia_agent_status => req is outstanding, value: 0x10
2. Address: 0x00000828 Name: region55_subregion2_cnr_if_snoc_uaxia_s_ta_agent_status => NO outstanding req, value:0x0
3. Address: 0x00000c28 Name: region55_subregion3_cnr_if_snoc_uaxib_m_ia_agent_status => NO outstanding req, value:0x0
4. Address: 0x00001028 Name: region55_subregion4_cnr_if_snoc_uaxib_s_ta_agent_status=> NO outstanding req, value:0x0
5. Address: 0x00001428 Name: region55_subregion5_cxram_csr_ta_agent_status => NO outstanding req, value:0x0
6. Address: 0x00001828 Name: region55_subregion6_lxb_snoc_daxi_s_ta_agent_status => NO outstanding req, value:0x0
7. Address: 0x00001c28 Name: region55_subregion7_lxb_snoc_daxia_m_ia_agent_status => NO outstanding req, value:0x0
8. Address: 0x00002028 Name: region55_subregion8_lxb_snoc_daxib_m_ia_agent_status=> NO outstanding req, value:0x0
9. Address: 0x00002428 Name: region55_subregion9_rt1_access_ta_agent_status => NO outstanding req, value:0x0
10. Address: 0x00002828 Name: region55_subregion10_soc_cip_pcie_data_ia_agent_status, req is outstanding, value: 0x50
11. Address: 0x00002c28 Name: region55_subregion11_soc_cip_sys_cfg_s_ta_agent_status, resp is active, value: 0x20
12. Address: 0x00003028 Name: region55_subregion12_soc_cip_sys_data_ia_agent_status, => NO outstanding req, value:0x0
13. Address: 0x00003428 Name: region55_subregion13_soc_cxram0_ta_agent_status => NO outstanding req, value:0x0
14. Address: 0x00003828 Name: region55_subregion14_soc_cxram1_ta_agent_status => NO outstanding req, value:0x0
15. Address: 0x00003c28 Name: region55_subregion15_soc_cxram2_ta_agent_status => NO outstanding req, value:0x0
16. Address: 0x00004028 Name: region55_subregion16_soc_cxram3_ta_agent_status => NO outstanding req, value:0x0
17. Address: 0x00004428 Name: region55_subregion17_soc_dbg_smb_m_ia_agent_status => NO outstanding req, value:0x0
18. Address: 0x00005428 Name: region55_subregion21_soc_dbg_smb_s_ta_agent_status => NO outstanding req, value:0x0
19. Address: 0x00005828 Name: region55_subregion22_soc_dbg_trace_sram_ta_agent_status => NO outstanding req, value:0x0
20. Address: 0x00005c28 Name: region55_subregion23_soc_if_csr_ta_agent_status => NO outstanding req, value:0x0

soc_noc_rt1=>{0x3E02_8000 to 0x3E02_C000 }

21. Address: 0x00000028 Name: region8_subregion0_lxb_snoc_daxi_s_ia_agent_status
22. Address: 0x00000428 Name: region8_subregion1_lxb_snoc_daxia_s_ta_agent_status
23. Address: 0x00000828 Name: region8_subregion2_lxb_snoc_daxib_s_ta_agent_status
24. Address: 0x00001028 Name: region8_subregion4_rt1_access_ia_agent_status, req is outstanding, value: 0x10

Functional monitoring for actionable insights

```
2455243,xbm5,161835558316,Y,axi monitor port 0,type:read_addr(direct),differentiator:0x1,tracker:0x1,addr:0x41E0BE18,burst:0x1,cache:0xB,id:0x53,len:0
x0,lock:0x0,prot:0x0,size:0x2
2455246,xbm5,161835558381,Y,axi monitor port 0,type:read_data,differentiator:0x1,tracker:0x2,data:0x325B203A61696266203E666E693C205D,id:0x6A,last:0x1,
resp:0x0
2455247,xbm5,161835623871,Y,axi monitor port 0,type:read_addr(direct),differentiator:0x1,tracker:0x2,addr:0x20F03FC0,burst:0x1,cache:0xB,id:0x6A,len:0
x0,lock:0x0,prot:0x0,size:0x4
01: 2455250,xbm5,161835623967,Y,axi monitor port 0,type:read_data,differentiator:0x1,tracker:0x1,data:0xB0000000000000000000000000000000000000000000000000
000,id:0x53,last:0x1,resp:0x0
01: 2455251,xbm5,161835624406,Y,axi monitor port 0,type:read_addr(direct),differentiator:0x0,tracker:0x1,addr:0x20F03FD0,burst:0x1,cache:0xB,id:0x7,len:0x
0,lock:0x0,prot:0x0,size:0x6
01: 2455288,xbm5,177493478730,Y,axi monitor port 0,flag:state_change,channel:write_data,enabled:0,history_mode:stream
2455289,xbm5,177493478730,Y,axi monitor port 0,flag:state_change,channel:read_data,enabled:0,history_mode:stream
01: 2455290,xbm5,177493478730,Y,axi monitor port 0,flag:state_change,channel:write_response,enabled:0,history_mode:stream
2455291,xbm5,177493478730,Y,axi monitor port 0,flag:state_change,channel:write_addr(direct),enabled:0,history_mode:stream
0:0 2455293,xbm5,177493478730,Y,axi monitor port 0,flag:state_change,channel:read_addr(direct),enabled:0,history_mode:stream
<END>
```


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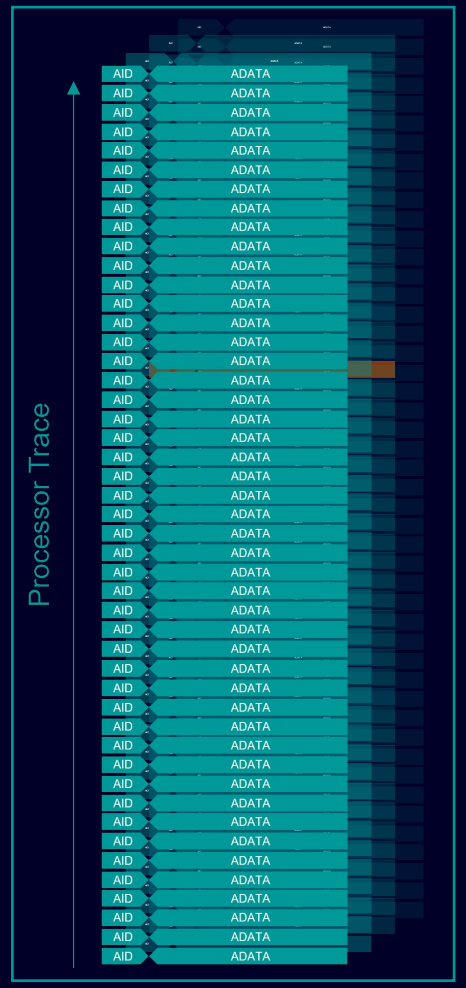
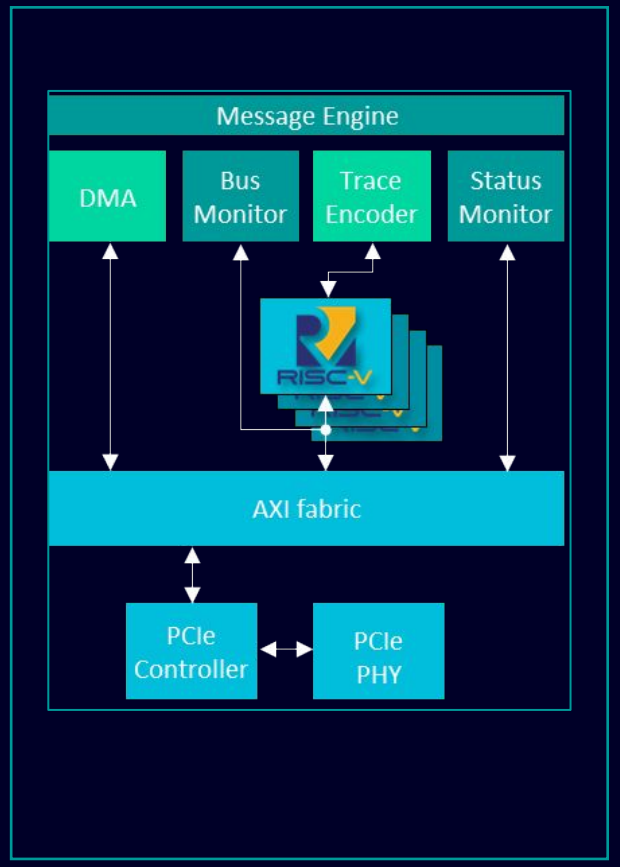
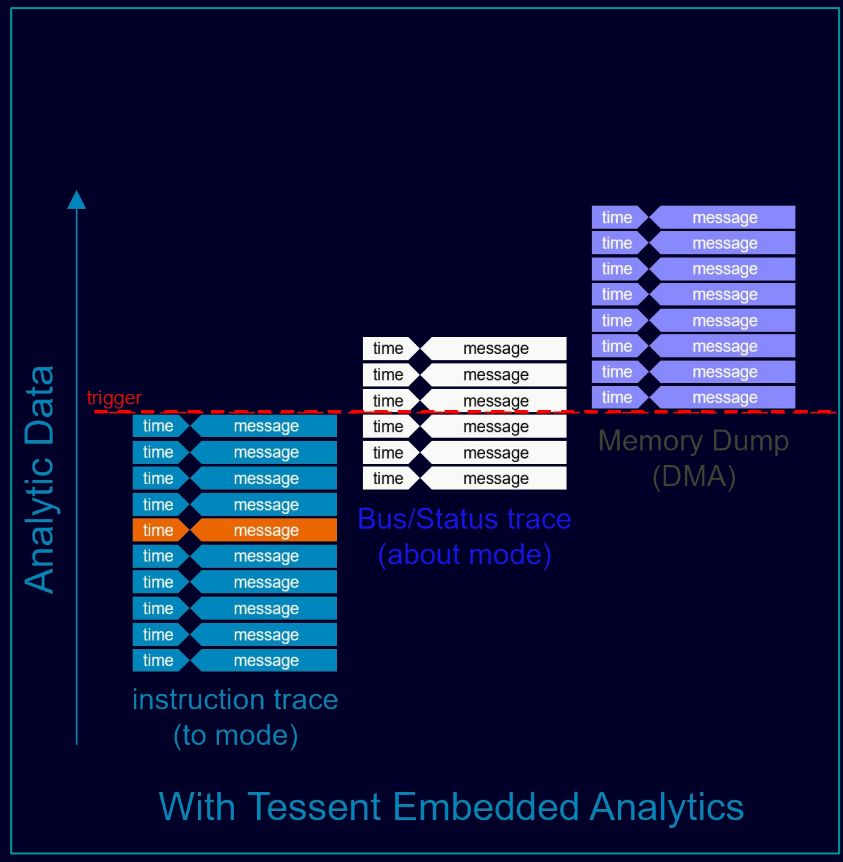
Functional monitoring for actionable insights



Traditional methods produce very large amount of trace data



SoC instrumented with Embedded Analytics IP



Capture relevant data around trigger condition Debug trace before, during and after failure

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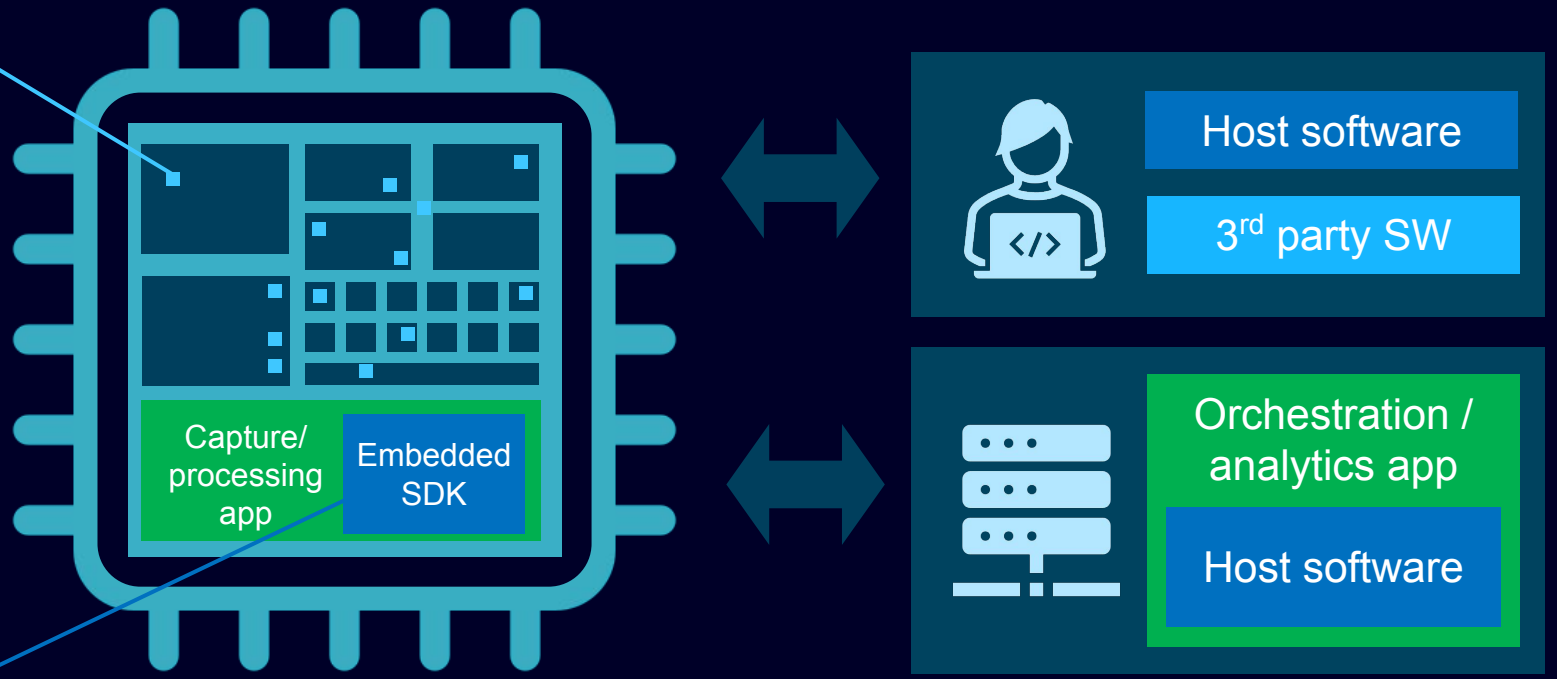
Building a Scalable SLM Solution

1 Smart monitors

2 Software for interactive debug and optimization



3 Edge analytics enablement

4 Fleet monitoring enablement

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Summary

Functional monitoring reduces debug time

Added visibility simplifies performance optimization

Smart functional monitoring helps save bandwidth

End-to-end, from bring-up to in-life

Visit Booth #30

Join us at RISC-V Europe Summit 2025

Presentation

Efficient debug and trace of RISC-V systems: a hardware/software co-design approach

Thursday May 15, 10:00 in Gaston Berger (S2)

Poster session available at Thursday May 15, Island 1.1 (S1)

Presentation

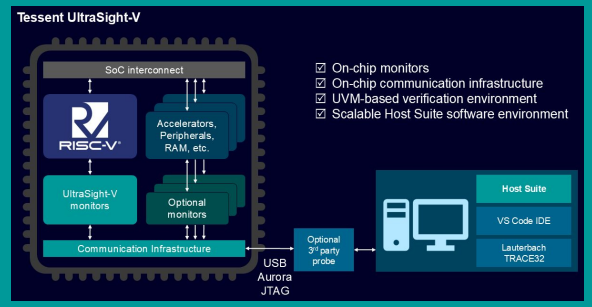
Unleashing the Power of RISC-V E-Trace with a Highly Efficient Software Decoder

Thursday May 15, 11:45 in Gaston Berger (S2)

Poster session available at Thursday May 15, Island 2.2 (S2)

Demo presentation

RISC-V on-chip debug & trace solution: Tessent UltraSight-V



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